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IQE plc

UNITED STATES DISTRICT COURT

CENTRAL DISTRICT OF CALIFORNIA

SOUTHERN DIVISION

IQE plc,

Plaintiff,

v.

NEWPORT FAB, LLC d/b/a JAZZ SEMICONDUCTOR, TOWER U.S. HOLDINGS INC., TOWER SEMICONDUCTOR LTD., PAUL D. HURWITZ, EDWARD PREISLER, DAVID J. HOWARD, and MARCO RACANELLI,

Defendants.

CASE NO. 8:22-cv-00867 CJC (KESx)
Judge Cormac J. Carney

CORRECTED **COMPLAINT FOR:**

(1) VIOLATION OF DEFEND TRADE SECRETS ACT

(2) VIOLATION OF CALIFORNIA UNIFORM TRADE SECRETS ACT

(3) CORRECTION OF INVENTORSHIP

(4) BREACH OF CONTRACT

(5) VIOLATION OF CALIFORNIA UNFAIR COMPETITION ACT

(6) INTENTIONAL INTERFERENCE WITH PROSPECTIVE ECONOMIC ADVANTAGE

(7) NEGLIGENT INTERFERENCE WITH PROSPECTIVE ECONOMIC ADVANTAGE

DEMAND FOR JURY TRIAL

Plaintiff IQE plc (IQE), for its complaints against Newport Fab, LLC, Tower U.S. Holdings Inc., Tower Semiconductor Ltd., Paul D. Hurwitz, Edward Preisler, David J. Howard, and Marco Racanelli (collectively, "Tower"), alleges as follows:[1]

NATURE OF THIS ACTION

1. This is an action for claims of misappropriation of IQE's trade secrets under both the Federal Defend Trade Secrets Act and the California Uniform Trade Secrets Act over Tower's unauthorized use of trade secrets covered by a mutually binding non-disclosure agreement (NDA) between IQE and Tower (Exhibit 1).

2. This action also encompasses a claim for correction of inventorship, under 35 U.S.C. § 256, of U.S. Patent Nos. 11,164,740 (the '740 patent) (Exhibit 2), 11,195,920 (the '920 patent) (Exhibit 3), 11,145,572 (the '572 patent) (Exhibit 4), and U.S. Patent Application 17/400,712 (the '712 application) (Exhibit 5), stemming from theft of IQE's inventions and trade secrets, which formed the basis for the claimed technology.

3. IQE also seeks relief for breach of contract under the aforementioned NDA.

4. IQE brings a claim of unfair competition under the Unfair Competition Law of California. C.A. Bus. & Prof. Code § 17200.

5. Finally, this action also brings a claim for intentional interference with prospective economic advantage, as well as a claim of negligent interference with economic advantage, because Tower's disclosure of IQE's trade secrets in Tower's patents and application wrongfully damaged IQE's relationships with potential customers and market position. *See* 28 U.S.C. § 167; *see also* Cal. Civ. Code § 3426.

[1] IQE's Complaint (ECF 1) attached the wrong document as Exhibit 4. This Corrected Complaint attached the proper document as Exhibit 4.

PARTIES

6. IQE plc is a British corporation that has its head office at Pascal Close, St Mellons, Cardiff, CF3 0LW, UK, where it was also incorporated. IQE plc operates several U.S. manufacturing sites directly or indirectly through its subsidiaries.

7. On information and belief, Newport Fab, LLC is a corporation organized under the laws of Delaware with its principal place of business at 4321 Jamboree Road, Newport Beach, California. In 2019, Newport Fab, LLC did business under the names "Jazz Semiconductor" and "TowerJazz."

8. On information and belief, Newport Fab, LLC, is indirectly held by Tower Semiconductor Newport Beach, Inc., itself indirectly held by Tower Semiconductor NPB Holdings, Inc. Both of these holding companies are organized under the laws of Delaware and share the office at 4321 Jamboree Road, Newport Beach, California, 92660 with Newport Fab, LLC.

9. On information and belief, these companies are themselves held directly and are controlled by Tower U.S. Holdings Inc., a corporation organized under the laws of Delaware. Tower U.S. Holdings Inc. thus acts in this forum through its subsidiaries and holdings. It is the agent of service for Tower Semiconductor Ltd., and its principal office is 2570 North First Street, Suite 480 San Jose, California, 95131.

10. On information and belief, Tower Semiconductor Ltd. is the parent company that directly holds Tower U.S. Holdings Inc. and controls and directs Newport Fab, LLC. Tower Semiconductor Ltd. thus acts in this forum through its subsidiaries and holdings. Tower Semiconductor Ltd. is an Israeli company with its head offices in the Ramat Gavriel Industrial Park, Shaul Amor Street, Post Office Box 619, Migdal Haemek, 2310502 Israel.

11. On information and belief, Paul D. Hurwitz was a former director of technology development at Newport Fab, LLC during the relevant period in 2018-

2020. He currently works as the Director of Foundry Engineering at Rockley Photonics Inc. He is domiciled in Irvine, California.

12. On information and belief, Edward Preisler is a current director of technology development at Newport Fab, LLC, and had this position during his involvement with IQE in the relevant period in 2018-2020. He is domiciled in San Clemente, California.

13. On information and belief, Dr. David J. Howard is an executive director and fellow of Tower Semiconductor Ltd. and had this position during his involvement with IQE in the relevant period in 2018-2020. He is domiciled in Newport Beach, California.

14. On information and belief, Marco Racanelli is the senior vice president and general manager of Newport Fab, LLC, and had this position during his involvement with IQE in the relevant period in 2018-2020. He is domiciled in Santa Ana, California.

JURISDICTION AND VENUE

15. This is a civil action seeking damages, injunctive relief, and other equitable relief under an action for correction of inventorship, 35 U.S.C. § 256, the Defend Trade Secrets Act, 18 U.S.C. § 1836, and California statutory and common law.

16. This Court has subject matter jurisdiction over this case pursuant to 28 U.S.C. § 1331 and 18 U.S.C. § 1836(c), as it involves actions arising under the laws of the United States. This Court has supplemental jurisdiction over the state law claims under 28 U.S.C. §1367, as they are so related to the federal claims as to form a single case.

17. Tower resides within the Central District of California and is subject to personal jurisdiction in the State of California because the unlawful conduct occurred in, and causes injuries in, California and this district specifically and because Tower (a) has signed an NDA that specifies the law and venue of

California as the proper jurisdiction, (b) has directed their activities concerning IQE, including the misappropriation of IQE's trade secrets, in California and this district, (c) transacts business in California, including operating a branch corporation in this district, (d) enters into contracts and partnerships with individuals and entities in this district, and (e) offers products and services for sale in this district.

18. Venue is proper in this district pursuant to 28 U.S.C. § 1391(b) because this is a district in which a substantial portion of the events giving rise to the claims occurred and in which IQE's injuries were suffered, as set forth below.

BACKGROUND

19. Since its founding in 1988, IQE has been the leading innovator and supplier of advanced wafer products, which are central to a broad range of downstream technologies, such as semiconductor devices, transistors (e.g., high electron mobility transistors (HEMTs), BiHEMTs, pseudomorphic high electron mobility transistors (pHEMTs), heterojunction bipolar transistors (HBTs), and bipolar field-effect transistors (BiFETs)), passive components, complementary metal-oxide-semiconductor (CMOS) processing, photonic devices, wireless devices, and radio frequency (RF) devices (e.g., RF switches and RF filters).

20. IQE's business model is unique in the industry, as IQE possesses processes to develop custom, individualized solutions to meet its customers' needs. These processes are a closely guarded trade secret, which has granted IQE a dominant position as a market innovator. IQE's unique capabilities were what drew Tower to pursue an exclusive licensing deal with IQE relating to IQE's porous silicon and epitaxial technologies.

21. IQE is the world's leading advanced wafer manufacturer and supplier and is the largest pure-play compound semiconductor wafer supplier with capability for volume manufacture across all semiconductor materials, including chemical vapor deposition (CVD), molecular beam epitaxy (MBE) and metal-organic

chemical vapor deposition (MOCVD) reactors for a variety of custom semiconductors.

22. IQE specializes in, among other applications, advanced Group IV and compound Group III-V semiconductors (e.g., silicon (Si), germanium (Ge), silicon germanium (SiGe), gallium arsenide (GaAs), indium phosphide (InP), gallium nitride (GaN), gallium antimonide (GaSb), indium antimonide (InSb), and multi-element alloys), including porous semiconductors. IQE also specializes in advanced semiconductor wafers utilized in wireless and RF products, such as transistors and switches, including epitaxy on porous silicon wafers as an alternative to silicon-on-insulator (SOI)-based devices. IQE's custom porous epitaxial wafers can be used for advanced microelectronics, optoelectronics, photonics, sensing, and high-performance RF and radiation-sensitive applications.

23. Tower is another figure in the semiconductor industry, known for the creation of specialized integrated circuits that are fabricated using wafers of the kind that IQE makes.

A. IQE's Business Model and Proprietary Information

24. IQE plc is a British semiconductor company founded in 1988; it also operates in the United States through subsidiaries in Pennsylvania, Massachusetts, North Carolina, and Washington.

25. Since its founding, IQE has been an industry leader in the manufacture of advanced epitaxial wafers and materials technologies used in a broad range of downstream technologies. In addition to manufacturing ready-made wafers, IQE also creates customized semiconductor solutions to meet its customers' specific needs. It is a one-stop-shop for the advanced Group IV and compound Group III-V semiconductor wafer needs of the world's leading semiconductor manufacturers.

26. To maintain its market position as a leader and innovator on a number of fronts, IQE protects a range of intellectual property pertaining both to the individual products it produces and sells and also the methods by which it develops

semiconductor solutions—including RF solutions. While IQE obtains patents on certain products and technologies, many of the processes that are crucial to its competitive advantage are kept as trade secrets. This is due to the difficulty in policing patents to processes and due to IQE's business model of contracting with customers for custom product solutions.

27. IQE's porous silicon technology is a superior alternative to high-resistivity silicon-on-insulator (SOI) substrates with a trap-rich layer. Porous silicon can achieve high-resistivity properties on a standard silicon CMOS wafer, rather than an SOI wafer. IQE's porous silicon technology produces comparable or better device performance than the previous SOI technology, is a simpler manufacturing process and has the additional advantage of using only a standard low-resistivity silicon CMOS substrate rather than a high-resistivity SOI substrate. Further, porous silicon can be thick enough to fully trap fringing fields, which significantly improves performance of devices fabricated on the porous silicon structure.

28. In 2018, based on these innovations, IQE began developing additional applications and products using its innovative porous silicon technology, which had the ability to outperform the competition. One such potential application that looked particularly promising was developing a high-performance RF switch using IQE's porous silicon technology. Another promising potential application was developing localized patterned porous segments, with adjacent porous and non-porous segments, combining IQE's porous silicon technology with RF switch technology.

B. Past Business Relations

29. On November 12, 2015, IQE and Tower entered into a mutually binding Non-Disclosure Agreement (NDA) as to any confidential information they disclose to one another as part of their business transactions. That NDA is attached as Exhibit 1 to this Complaint and is incorporated by reference. The NDA protects "all information, documents, data, reports, interpretations, forecasts, analyses, compilations, studies, ideas, inventions (whether or not patentable), trade secrets

and works of authorship, proprietary information, or records of or concerning the disclosing party or its affiliates, provided by the disclosing party to the receiving party, as well as all information in tangible form that bears a 'confidential,' 'proprietary,' 'secret,' or similar legend and discussions of that information relating to that information whether those discussions occur prior to, concurrent with, or following the disclosure of the information." Exhibit 1. The NDA also specifies the proper venue and law for any dispute "[t]his agreement, as well as any disputes arising out of or relating to this agreement, shall be interpreted under and governed by the laws of the State of California. Any disputes arising out of or relating to this Agreement and not resolved by the parties themselves shall be commenced solely in the Federal or state courts located within the State of California. In such event, each party irrevocably agrees to submit to the personal jurisdiction of such courts and waives any objection to such venue." *Id.*

C. IQE Approaches Tower about a Potential Collaboration

30. In November 2018, IQE and Tower began discussing a potential collaboration providing IQE's porous silicon technology with Tower's RF sensor technology to create new semiconductor products.

31. As a part of the parties' mutual exploration of a potential collaboration, Tower requested, and IQE provided, proprietary trade secrets pertaining to IQE's porous silicon and crystalline epitaxy wafers. For example, on November 6, 2018, IQE presented its epitaxy on porous silicon technology to Tower, followed by sending a copy of the presentation given with additional information and background papers. And, on July 24, 2019, IQE presented its epitaxy on porous silicon technology for RF switches to Tower, followed by sending a copy of the presentation given. Copies of these presentations are attached as Confidential Exhibits 6 and 7, respectively, and are incorporated by reference. Formal presentations were not the only times IQE shared information on their trade secrets

as they also furnished Tower with emails answering specific questions about IQE's capabilities, technical papers, and experimental data. *See* Confidential Exhibit 8, 9.

32. All of these meetings and presentations, and the information exchanged therein, were protected by the mutually binding NDA signed by the parties in November 2015. Because the information at issue contained IQE's highly valuable and important trade secrets, IQE took additional steps prior to these meetings to remind Tower of its ongoing obligation under that NDA not to use or disclose any information conveyed without IQE's consent. This obligation included "all information, documents, data, reports, interpretations, forecasts, analyses, compilations, studies, ideas, inventions (whether or not patentable), trade secrets and works of authorship, proprietary information, or records of or concerning the disclosing party or its affiliates, provided by the disclosing party to the receiving party, as well as all information in tangible form that bears a 'confidential,' 'proprietary,' 'secret,' or similar legend and discussions of that information relating to that information whether those discussions occur prior to, concurrent with, or following the disclosure of the information." Exhibit 1. All slides that IQE representatives displayed during these meetings and presentations were clearly marked as containing highly confidential information proprietary to IQE. *See* Confidential Exhibit 6, 7.

33. Due to IQE's innovative processes and technology, Tower displayed a strong interest in IQE's porous silicon technology and proposed a contract for a multi-year supply agreement. One of the terms of Tower's proposed Memorandum of Understanding ("MOU") was a multi-year period of exclusivity, during which IQE could not supply any other customer with its porous silicon technology solutions. This MOU is attached to this complaint and incorporated by reference as Confidential Exhibit 11. *See also* Confidential Exhibit 10.

34. IQE was not willing to forego selling one of its flagship innovations to other customers, and it counter-offered that it would enter into a non-exclusive partnership with Tower with a preferential pricing scheme.

35. This led to an impasse in negotiations as Tower insisted in an email on October 21, 2019, that exclusivity would need to exist in order for any deal to go forward. A true copy of this email is attached as Confidential Exhibit 10 and is incorporated by reference.

36. Ultimately, Tower's strong desire to exclusively practice IQE's proprietary technology, and the failure to align on a mutually acceptable preferential pricing scheme, caused a breakdown in negotiations. On February 24, 2020, IQE and Tower concluded that the planned collaboration could not go forward and agreed to end negotiations.

D. Tower Pursues Exclusive Rights to IQE's Porous Silicon Technology

37. On October 9, 2019—less than three weeks after presenting IQE with a draft memorandum of understanding that granted Tower a three-year period of exclusivity and only six weeks after IQE disclosed their invention for porous semiconductor layers for RF devices—Tower filed a patent application on "Semiconductor Structure Having Porous Semiconductor Layer for RF Devices." Tower secretly copied into their patent application IQE's trade secret information that was communicated to Tower during the parties' confidential meetings. This application would eventually be granted as the '740 patent. A copy of the '740 patent is attached as Exhibit 2 to this Complaint and is incorporated by reference.

38. The '740 patent names Paul Hurwitz, Edward Preisler, David Howard, and Marco Racanelli as inventors. *See* Exhibit 2. Each of these individuals was directly involved in the negotiations with IQE and either directly received and reviewed IQE's proprietary information during the confidential meetings or had access to it through subsequent discussions.

39. For example, Paul Hurwitz attended the confidential meeting on the scope of the proposed joint development. He defined the desired specifications for the porous silicon samples and requested follow-up information.

40. Edward Preisler participated in several confidential discussions regarding the different types of porous substrate development at IQE. David Howard also participated in the confidential discussions, was privy to confidential information, and observed the progress of the porous silicon discussion specifically.

41. Marco Racanelli was a senior vice president of Tower and oversaw much of the negotiations. Marco Racanelli gave specific directives to the other Tower employees on what to negotiate for, and at times Marco Racanelli negotiated directly with IQE. On September 13, 2019, a month before Tower began filing patents derived from IQE's intellectual property, Marco Racanelli emailed Wayne Johnson, head of wireless business development at IQE, to state that Tower had a need for IQE's porous silicon technology and were under a time pressure to make an agreement.

42. All claims of the '740 patent recite the porous semiconductor technology developed by IQE. The entirety of the invention claimed in the '740 patent was therefore derived from IQE's trade secrets conveyed to Tower during negotiations and discussions between the parties.

43. Specifically, at least claims 1-4, 8-11, 14, 15, and 17-19 of the '740 patent recite proprietary trade secrets that IQE communicated to Tower:

(a) For example, claim 1 of the '740 patent recites: "A semiconductor structure comprising: a substrate having a first dielectric constant; a porous semiconductor layer situated over said substrate; at least one crystalline epitaxial layer situated directly on said porous semiconductor layer; a first semiconductor device situated in said at least one crystalline epitaxial layer; said porous semiconductor layer having a second dielectric constant that is substantially

less than said first dielectric constant such that said porous semiconductor layer reduces signal leakage from said first semiconductor device." *See* Exhibit 2.

(b) Claim 4 of the '740 patent recites: "The semiconductor structure of claim 1, wherein said first semiconductor device is a transistor utilized in a radio frequency (RF) switch." *Id.*

(c) Claim 8 of the '740 patent recites: "A semiconductor structure comprising: a porous silicon layer; at least one crystalline epitaxial layer situated directly on said porous silicon layer; first and second transistors situated in said at least one crystalline epitaxial layer; an electrical isolation region separating said first and second transistors." *Id.*

(d) Claim 9 of the '740 patent recites: "The semiconductor structure of claim 8, wherein said porous silicon layer is situated over a bulk silicon substrate." *Id.*

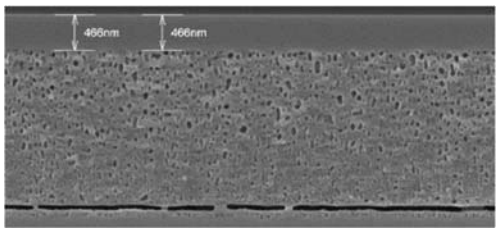
(e) Claim 11 of the '740 patent recites: "The semiconductor structure of claim 8, wherein said first transistor is utilized in a radio frequency (RF) switch." *Id.*

(f) Claim 14 of the '740 patent recites: "A semiconductor structure comprising: a porous semiconductor layer situated over a substrate, said porous semiconductor layer having a higher resistivity than said substrate; at least one crystalline epitaxial layer situated directly on said porous semiconductor layer; a first semiconductor device situated in said at least one crystalline epitaxial layer." *Id.*

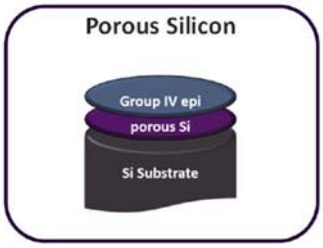
(g) Claim 15 of the '740 patent recites: "The semiconductor structure of claim 14, wherein said substrate comprises a first semiconductor material, and said porous semiconductor layer comprises said first semiconductor material." *Id.*

(h) Claim 19 of the '740 patent recites: "The semiconductor structure of claim 14, wherein said first semiconductor device is a transistor utilized in a radio frequency (RF) switch." *Id.*

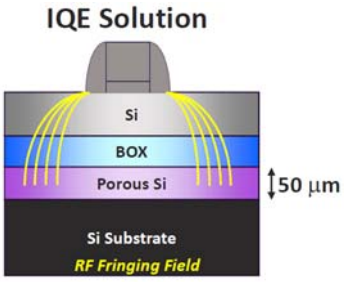
44. The form and function of the semiconductor structures contemplated by the '740 patent and recited in its claims are identical to the porous semiconductor structures that are based on IQE's proprietary porous silicon technology. For example, in IQE's confidential presentations to Tower on November 6, 2018 ("2018 Presentation") and on July 24, 2019 ("2019 Presentation"), IQE presented examples of IQE's porous silicon technology, epitaxy on porous silicon, and applications for RF devices, including diagrams and



Confidential Exhibit 6, Pg. 9



Confidential Exhibit 7, Pg. 11



Confidential Exhibit 7, Pg. 14

explanations of IQE's methodology and advantages over the competition, which are substantively similar to Tower's claims in the '740 patent. Indeed, the 2019 Presentation stated "[p]orous Si for RF Switches…[s]ignificantly improved harmonics…[n]o change in device architecture." (Confidential Exhibit 7, Pg. 14.)

45. On October 10, 2019, Tower applied for a second patent—the '920 patent—naming the same inventors as the '740 patent and further misappropriating IQE's trade secrets in its claims. All claims of the '920 patent recite porous semiconductor technology developed by IQE. The entirety of the invention claimed in the '920 patent was therefore derived from IQE's trade secrets conveyed to Tower during negotiations and discussions between the parties. A copy of the '920 patent is attached as Exhibit 3 to this Complaint and is incorporated by reference.

46. Specifically, at least claims 1-6, 8-12, 14-17, and 19 of the '920 patent claim proprietary trade secrets that IQE communicated to Tower and the named inventors:

(a) For example, claim 1 of the '920 patent recites: "A semiconductor structure comprising: a porous semiconductor segment adjacent to a first region of a substrate; at least one crystalline epitaxial layer situated over said porous semiconductor segment and over said first region of said substrate; a first semiconductor device situated in said at least one crystalline epitaxial layer over said porous semiconductor segment; a second semiconductor device situated in said at least one crystalline epitaxial layer over said first region of said substrate but not over said porous semiconductor segment; said first region of said substrate having a first dielectric constant, and said porous semiconductor segment having a second dielectric constant that is substantially less than said first dielectric constant such that said porous semiconductor segment reduces signal leakage from said first semiconductor device." *See* Exhibit 3.

(b) Claim 2 of the '920 patent recites: "The semiconductor structure of claim 1, wherein a second region of said substrate is situated under said porous semiconductor segment and under said first region of said substrate." *Id.*

(c) Claim 5 of the '920 patent recites: "The semiconductor structure of claim 1, wherein said first semiconductor device is a transistor utilized in a radio frequency (RF) switch." *Id.*

(d) Claim 8 of the '920 patent recites: "A semiconductor structure comprising: a porous silicon segment adjacent to a first region of a bulk silicon substrate; at least one crystalline epitaxial layer situated over said porous silicon segment and over said first region of said bulk silicon substrate; a first transistor situated in said at least one crystalline epitaxial layer over said porous silicon segment; a second transistor situated in said at least one crystalline epitaxial layer over said first region of said bulk silicon substrate but not over said porous silicon

segment; an electrical isolation region separating said first and second transistors." *Id.*

(e) Claim 11 of the '920 patent recites: "The semiconductor structure of claim 8, wherein said first transistor is utilized in a radio frequency (RF) switch." *Id.*

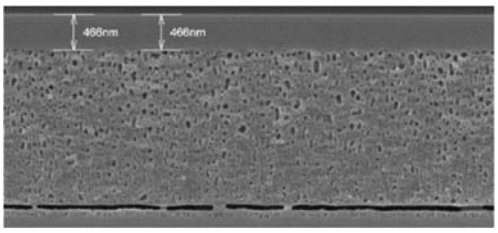
(f) Claim 14 of the '920 patent recites: "A semiconductor structure comprising: a porous silicon segment adjacent to a bulk silicon substrate; at least one crystalline epitaxial layer having a first region situated over said porous silicon segment; said at least one crystalline epitaxial layer having a second region situated over said bulk silicon substrate but not over said porous silicon segment; an electrical isolation region separating said first region of said at least one crystalline epitaxial layer from said second region of said at least one crystalline epitaxial layer." *Id.*

(g) Claim 16 of the '920 patent recites: "The semiconductor structure of claim 14, wherein a first semiconductor device is situated in said first region of said at least one crystalline epitaxial layer and a second semiconductor device is situated in said second region of said at least one crystalline epitaxial layer." *Id.*

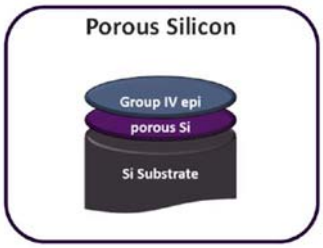
(h) Claim 19 of the '920 patent recites: "The semiconductor structure of claim 16, wherein said first semiconductor device is a first transistor that is utilized in a radio frequency (RF) switch." *Id.*

47. The form and function of the semiconductor structures contemplated by the '920 patent and recited in its claims were devised as part of the collaboration with IQE, and which are based on IQE's proprietary porous silicon technology. For example, in IQE's confidential 2018 Presentation and 2019 Presentation to Tower, IQE presented examples of IQE's porous silicon technology, CMOS compatible epitaxy on porous silicon, and applications for localized RF devices, including diagrams and explanations of IQE's methodology and advantages over the

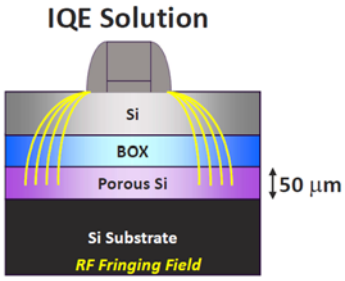
competition, which are substantively similar to Tower's claims in the '920 patent. Indeed, in a correspondence between Richard Hammond of IQE and Edward



Confidential Exhibit 6, Pg. 9



Confidential Exhibit 7, Pg. 11



Confidential Exhibit 7, Pg. 14

Preisler of Tower on November 7, 2018, Richard Hammond proposed a "[l]ocalized porous demonstrator…to expose localized areas for subsequent thick porous silicon formation…[i]nductors on selective porous regions." (Confidential Exhibit 9, Pg. 1.)

48. Furthermore, a stated goal of the '920 patent is to create semiconductor dies with "reduced RF signal leakage, reduced need for numerous body contacts, and increased heat dissipation at low cost." Exhibit 3. These include advantages presented by IQE to Tower during at least one of the confidential meetings between the parties. For example, their 2019 Presentation describes suppressing a "RF fringing field" due to properties of the porous layer that had "[s]ignificantly improved harmonics" and "[i]mproved cross talk compared to Trap-rich HR-Si." (Confidential Exhibit 7, Pgs. 14-15.) Improved signal leakage was one of the expected benefits from the collaboration.

49. IQE's inventors of the porous silicon technology continued to share positive test results with Tower. The mutual NDA was still in place during these conversations, as Tower and IQE were considering collaborations for other projects.

50. On December 4, 2019, Tower applied for a third patent related to IQE's porous silicon technology—the '572 patent—naming David J. Howard as the sole inventor. The '572 patent is attached as Exhibit 4 to this Complaint and is incorporated by reference. The very next day, David Howard emailed IQE

employees, including Wayne Johnson, asking for further meetings and information and noting that David Howard had been "observing progress on porous Si discussions" on an ongoing basis.

51. The '572 patent sought to leverage porous silicon to "withstand thermal and mechanical stresses" and further misappropriated IQE's trade secrets in its claims. Exhibit 4. All claims of the '572 patent recite porous semiconductor technology developed by IQE. The entirety of the invention claimed in the '572 patent was therefore derived from IQE's trade secrets conveyed to Tower during negotiations between the parties.

52. Specifically, at least claims 1, 2, 13, and 14 of the '572 patent claim proprietary trade secrets that IQE communicated to Tower and the named inventor:

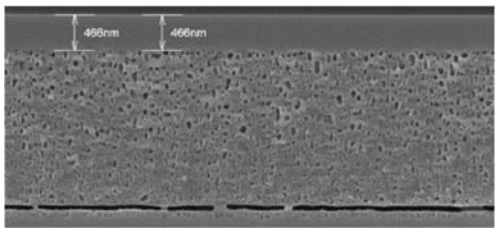
(a) For example, claim 1 of the '572 patent recites: "A semiconductor structure comprising: a semiconductor substrate; a porous semiconductor region within said semiconductor substrate, wherein said porous semiconductor region is not a dielectric material; a through-substrate via (TSV) within said porous semiconductor region; said porous semiconductor region causing said semiconductor structure and/or said TSV to withstand thermal and mechanical stresses." Exhibit 4.

(b) Claim 2 of the '572 patent recites: "The semiconductor structure of claim 1, wherein said porous semiconductor region has a first coefficient of thermal expansion (CTE) that is significantly greater than a second CTE of said semiconductor substrate." *Id.*

(c) Claim 13 of the '572 patent recites: "A semiconductor structure comprising: a semiconductor substrate; a porous semiconductor region within said semiconductor substrate, wherein said porous semiconductor region is not a dielectric material; a through-substrate via (TSV) at least partially within said porous semiconductor region; said porous semiconductor region causing said semiconductor structure to withstand thermal or mechanical stress." *Id.*

(d) Claim 14 of the '572 patent recites: "The semiconductor structure of claim 13, wherein said porous semiconductor region has a first coefficient of thermal expansion (CTE) that is greater than a second CTE of said semiconductor substrate." *Id.*

53. The form and function of the semiconductor structures contemplated



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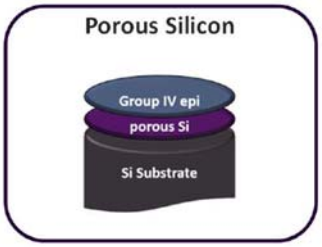
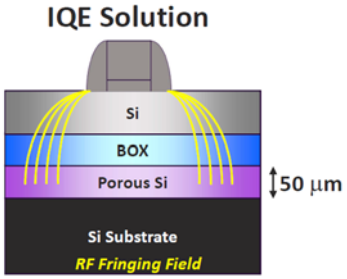


Confidential Exhibit 7, Pg. 11



Confidential Exhibit 7, Pg. 14

by the '572 patent and recited in its claims are based on IQE's proprietary porous silicon technology. For example, in IQE's confidential 2018 Presentation and 2019 Presentation to Tower, IQE presented examples of IQE's porous silicon technology, CMOS compatible epitaxy on porous silicon, and applications for RF devices, including diagrams and explanations of IQE's methodology and advantages over the competition, which are substantively similar to Tower's claims in the '572 patent. Indeed, the 2018 Presentation stated "CMOS Fab compatible" and the 2019 Presentation stated "CMOS Processing Compatible." *See* Confidential Exhibit 6, 7. Further, in a correspondence between Richard Hammond of IQE and Edward Preisler and Paul D. Hurwitz of Tower on November 13, 2018 ("2018 Response"), Richard Hammond discussed an "STI [shallow trench isolation] module…STI etch will consume the 1450A body and penetrate into the porous region." (Confidential Exhibit 9, Pg. 1.)

54. In addition, the MOU between the parties stated "[m]echanical strength is expected to be compromised Vs c-Si substrates, and the *large TCE mismatch* between c-Si [crystalline silicon] and p-Si [porous silicon] may limit thermal ramp

rates…may need to improve mechanical parameters such as bow and warp." *See* Confidential Exhibit 11.

55. On August 12, 2021, Tower once again applied for a patent based on IQE's trade secrets disclosed during the negotiations with IQE—the '712 application. This application seeks to patent methods of forming semiconductor structures using porous silicon in RF devices using the concepts initially disclosed to Tower by IQE. A copy of the '712 application is attached to this Complaint as Exhibit 5 and is incorporated by reference.

56. All claims of the '712 application thus recite porous semiconductor technology and methods developed by IQE. The entirety of the invention claimed in the '712 application was derived from IQE's trade secrets conveyed to Tower during negotiations between the parties.

57. Specifically, at least claims 14-19, 22-25, 27, 28, and 30-32 of the '712 application claim proprietary trade secrets that IQE communicated to Tower and the named inventor:

(a) For example, claim 14 of the '712 application recites: "A method comprising: forming a crystalline epitaxial layer over a porous semiconductor layer, said porous semiconductor layer being situated over a substrate; forming a first semiconductor device in said crystalline epitaxial layer; said substrate having a first dielectric constant, and said porous semiconductor layer having a. second dielectric constant that is substantially less than said first dielectric constant such that said porous semiconductor layer reduces signal leakage from said first semiconductor device." *See* Exhibit 5.

(b) Claim 15 of the '712 application recites: "The method of claim 14, further comprising annealing said porous semiconductor layer prior to said forming said crystalline epitaxial layer." *Id.*

(c) Claim 19 of the '712 application recites: "The method of claim 14, wherein said first semiconductor device is a transistor utilized in a radio frequency (RF) switch." *Id.*

(d) Claim 22 of the '712 application recites: "A method comprising: forming at least one crystalline epitaxial layer over a porous silicon layer in a semiconductor structure; forming first and second transistors and an electrical isolation region separating said first and second transistors in said at least one crystalline epitaxial layer." *Id.*

(e) Claim 23 of the '712 application recites: "The method of claim 22, further comprising forming said porous silicon layer over a bulk silicon substrate prior to said forming said at least one crystalline epitaxial layer." *Id.*

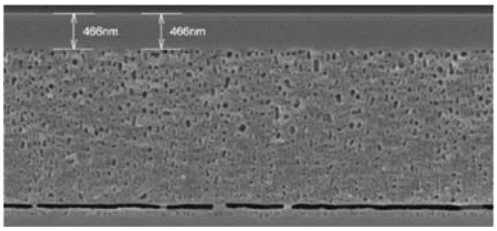
(f) Claim 27 of the '712 application recites: "A method comprising: forming a porous semiconductor layer over a substrate, said porous semiconductor layer having a higher resistivity that said substrate; forming at least one crystalline epitaxial layer over said porous semiconductor layer; forming a first semiconductor device in said at least one crystalline epitaxial layer." *Id.*

(g) Claim 28 of the '712 application recites: "The method of claim 27, wherein said substrate comprises a first semiconductor material, and said porous semiconductor layer comprises said first semiconductor material." *Id.*

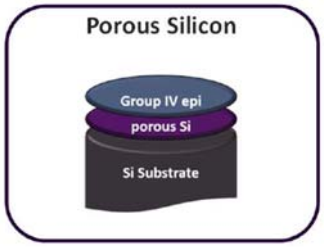
(h) Claim 32 of the '712 application recites: "The method of claim 27, wherein said first semiconductor device is a transistor utilized in a radio frequency (RF) switch." *Id.*

58. Similar to the '740 patent, the form and function of the semiconductor structures and methods contemplated by the '712 application and recited in its claims are identical to the porous semiconductor structures and methods which are IQE's proprietary porous silicon technology. For example, in IQE's confidential 2018 Presentation and 2019 Presentation to Tower, IQE presented examples of IQE's porous silicon technology, epitaxy on porous silicon, and applications for RF

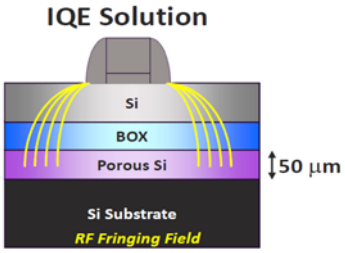
devices, including diagrams and explanations of IQE's methodology and advantages over the competition, which are substantively similar to Tower's claims



Confidential Exhibit 6, Pg. 9



Confidential Exhibit 7, Pg. 11



Confidential Exhibit 7, Pg. 14

in the '712 application. Indeed, the 2019 Presentation stated "[p]orous Si for RF Switches…[s]ignificantly improved harmonics…[n]o change in device architecture." (Confidential Exhibit 7, Pg. 14.)

59. In addition, the 2019 Presentation stated IQE's porous silicon technology was "CMOS Processing Compatible" and that there was "[n]o degradation with *annealing*." (Confidential Exhibit 7, Pg. 16 (emphasis added).) Moreover, in the 2018 Response, Richard Hammond of IQE stated "[t]he wafers that we provide will have undergone a *pre-epi flash off* [anneal] in excess of 1100C." (Confidential Exhibit 9, Pg. 1 (emphasis added).)

60. IQE was unaware of Tower's conduct until the patent applications were published. Tower never informed IQE that it filed these patent applications. Three of the patent applications were published on the same day April 15, 2021, and the remaining application, the '712 application, was published on December 2, 2021. IQE only found out about Tower's actions upon seeing these published applications.

61. Tower sought to secure an advantageous market system by entering into an exclusive contract with IQE, in order to benefit from IQE's trade secrets. Indeed, Tower insisted on exclusivity as essential to any supplier agreement with IQE. IQE's refusal to agree to that exclusivity contributed to the breakdown of the negotiations. *See* Confidential Exhibit 10.

62. Had Tower been the true inventor of the technology now claimed in its patents and application, it would not have needed exclusivity through contract. There is no reason to insist on contractual exclusivity where exclusive rights are secured through patents. Tower's behavior confirms that it did not believe itself to have exclusive rights to IQE's porous silicon technology.

63. Having been denied an exclusive deal with IQE, Tower now seeks to gain by deception what it could not gain through negotiation and contractual agreement. By using patent rights to gain exclusive rights to IQE's trade secrets, Tower looks to force IQE's hand, compelling it to deal with Tower—and Tower alone—in order to practice its own technology.

64. Since learning of Tower's patents directed to IQE's porous silicon technology, and thus Tower's misconduct, IQE has diligently pursued its legal interests, including by filing this Complaint.

COUNT I

Violation of the Defend Trade Secrets Act (18 U.S.C. § 1836 et seq.)

65. IQE incorporates by reference each and every allegation contained in paragraphs 1–64 above as if fully set forth herein.

66. Between October 2018 and February 2020, IQE and Tower were engaged in negotiations surrounding a potential collaboration between the two companies in which Tower repeatedly sought exclusive access to IQE's trade secrets including, but not limited to, the following: manufacture and use of porous silicon wafers, III-V materials on silicon-germanium alloys, rare earth material filters, and advanced III-V power devices.

67. During these negotiations, IQE provided Tower with information pertaining to a number of IQE trade secrets in the form of presentations, experimental data, and detailed descriptions of the composition of IQE's wafers.

68. On October 9, 2019, October 10, 2019, and December 4, 2019, while negotiations with IQE were still ongoing, Tower applied for the '740, '920, and '572 patents.

69. On August 12, 2021, Tower filed for another patent: the '712 application.

70. These patents and patent application all claim a "semiconductor structure comprising: . . . porous silicon," and recite in their specifications and claims proprietary trade secrets that Tower had obtained from the negotiations with IQE and under a duty of confidentiality.

71. This disclosure and use of IQE's trade secrets amounts to misappropriation under 18 U.S.C. § 1836(b)(1).

72. IQE took great care to safeguard its trade secrets, only disclosing them to IQE personnel and as needed for its legitimate business interests. Materials containing trade secrets were marked as confidential and kept secret. When disclosed to Tower, IQE took care to ensure they were only disclosed under a strict NDA. Moreover, IQE repeatedly reminded Tower of the receiver's obligation of confidentiality.

73. Tower has copied IQE's valuable trade secrets, incorporated them into Tower's patents and patent application, is using them, and intends to continue using them to further its business interests and to damage IQE's market standing.

74. IQE did not authorize or consent to Tower or anyone else using its trade secrets. IQE's disclosure of the protected information was strictly confidential and subject to an NDA. Tower was aware that it had received IQE's trade secrets and made clear that it understood that it was under an obligation not to disclose those secrets or appropriate the information therein for its own benefit.

75. Prior to the acts complained of herein, IQE's trade secrets had, and continue to have, independent economic value deriving from the fact that such information is not readily ascertainable through proper means nor known to IQE's

competitors, their customers, or the public at large who could obtain economic value from their use or disclosure.

76. Tower has used IQE's trade secrets to obtain patents on IQE's technology, including the '740, '920, and '572 patents, and the '712 application. This misappropriation has destroyed the secrecy of this information. Any enforcement of Tower's ill-gotten patents will prevent IQE from freely practicing its own technology. The existence of the patents themselves has an immediate and ongoing pronounced chilling effect on IQE's ability to market its technology to other customers.

77. The applications that issued as the '740, '920, and the '572 patents were published on April 15, 2021. The '712 application was published on December 2, 2021.

78. IQE discovered these patent applications, and thus discovered Tower's misappropriation of IQE's trade secrets, on February 14, 2022, as part of its routine diligence. IQE has brought this action within the three-year period prescribed by 18 U.S.C. § 1836(d), and its claims are not time barred.

79. As a direct and proximate result of Tower's misappropriation and use of IQE's trade secrets, IQE has suffered irreparable harm subject to proof at trial.

80. In addition to said damages, Tower has been unjustly enriched by its misappropriation and use of IQE's trade secrets.

81. Tower's misappropriation of IQE's trade secrets was willful and malicious, so as to justify an award of additional punitive damages pursuant to 18 U.S.C. § 1836(b)(3)(C), in a sum sufficient to punish Tower and deter others from engaging in similar misconduct.

82. Because the misappropriation by Tower was willful and malicious, IQE is also entitled to an award of reasonable attorney's fees and costs incurred during litigation pursuant to 18 U.S.C. § 1836 (b)(3)(D).

83. IQE is further entitled to an order enjoining Tower from further using IQE's trade secrets to unfairly compete with IQE, and to an order further compelling Tower to turn over to IQE all copies of IQE's trade secrets in their possession, custody, or control.

COUNT II:

Violation of California Trade Secrets Act (Cal. Civ. Code § 3246 et seq.)

84. IQE incorporates by reference each and every allegation contained in paragraphs 1–83 above as if fully set forth herein.

85. Between October 2018 and February 2020, IQE and Tower were engaged in negotiations surrounding a potential collaboration between the two companies in which Tower repeatedly sought exclusive access to IQE's trade secrets including, but not limited to, the following: manufacture and use of porous silicon wafers, III-V materials on silicon-germanium alloys, rare earth metal filters, and advanced III-V power devices.

86. During these negotiations, IQE provided Tower with information pertaining to a number of IQE trade secrets in the form of presentations, experimental data, and detailed technical description of the composition of IQE's wafers.

87. On October 9, 2019, October 10, 2019, and December 4, 2019, while negotiations with IQE were still ongoing, Tower applied for '740, '920, and '572 patents.

88. On August 12, 2021, Tower filed for another patent: the '712 application.

89. These patents and patent application all claimed a "semiconductor structure comprising: . . . porous silicon," and recite in their specifications and claims proprietary trade secrets that Tower obtained from the negotiations with IQE and under a duty of confidentiality.

90. This disclosure and use of IQE's trade secrets amounts to misappropriation under Cal. Civ. Code § 3426.1(b).

91. IQE took great care to safeguard its trade secrets, only disclosing them to IQE personnel and as needed for its legitimate business interests. Materials containing trade secrets were marked as confidential and kept secret. When disclosed to Tower, IQE took care to ensure they were only disclosed under a strict NDA. Moreover, IQE repeatedly reminded Tower of the receiver's obligation of confidentiality.

92. Tower has copied IQE's trade secrets, incorporated them into Tower's patents and patent application, is using them, and intends to continue using them to further their business interests and to damage IQE's market standing.

93. IQE did not authorize or consent to Tower or anyone else using its trade secrets. IQE's disclosure of the protected information was strictly confidential and subject to an NDA. Tower understood that it had received IQE's trade secrets and understood that it was under an obligation not to disclose those secrets or appropriate the information therein for its own benefit.

94. Prior to the acts complained of herein, IQE's trade secrets had, and continue to have, independent economic value deriving from the fact that such information is not readily ascertainable through proper means nor known to IQE's competitors, their customers, or the public at large who could obtain economic value from their use or disclosure.

95. Tower has used IQE's trade secrets in the patenting of the subject matter claimed in the '740, '920, and '572 patents, and the '712 application. The result of this misappropriation is to prevent IQE from practicing its own technology independently of Tower.

96. IQE discovered Tower's misappropriation of IQE's trade secrets in 2022, shortly after Defendant's patent applications were published in April and

December of 2021. IQE has brought this action within the three-year period prescribed by Cal. Civ. Code § 3426.6, and its claims are not time barred.

97. As a direct and proximate result of Tower's misappropriation and use of IQE's trade secrets, IQE has suffered irreparable damages in an amount exceeding the minimum jurisdictional limits of this Court and subject to proof at trial.

98. In addition to said damages, Tower has been unjustly enriched by the misappropriation and use of IQE's trade secrets.

99. Tower's misappropriation of IQE's trade secrets was willful and malicious, so as to justify an award of additional exemplary damages pursuant to Cal. Civ. Code § 3426.3(c), in a sum sufficient to punish Tower and deter other from engaging in similar misconduct.

100. Because the misappropriation by Tower was willful and malicious, IQE is also entitled to an award of reasonable attorney's fees and costs incurred during litigation pursuant to Cal. Civ. Code § 3426.4.

101. IQE is further entitled to an order enjoining Tower from further using IQE's trade secrets to unfairly compete with IQE, and to an order further compelling Tower to turn over to IQE all copies of IQE's trade secrets in their possession, custody, or control.

COUNT III:

Correction of Inventorship (35 U.S.C. § 256)

102. IQE incorporates by reference each and every allegation contained in paragraphs 1–101 above as if fully set forth herein.

103. Since beginning negotiations with IQE, Tower has applied for 4 patents relating to porous silicon semiconductors: the '740, '920, and '572 patents and the '712 application.

104. Claims 1 and 8 of the '740 patent are representative.

(a) Claim 1 recites: "A semiconductor structure comprising: a substrate having a first dielectric constant; a porous semiconductor layer situated over said substrate; at least one crystalline epitaxial layer situated directly on said porous semiconductor layer; a first semiconductor device situated in said at least one crystalline epitaxial layer; said porous semiconductor layer having a second dielectric constant that is substantially less than said first dielectric constant such that said porous semiconductor layer reduces signal leakage from said first semiconductor device." *See* Exhibit 2.

(b) Claim 8 recites: "A semiconductor structure comprising: a porous silicon layer; at least one crystalline epitaxial layer situated directly on said porous silicon layer; first and second transistors situated in said at least one crystalline epitaxial layer; an electrical isolation region separating said first and second transistors." *Id.*

105. These claims encompass the proprietary porous silicon and crystalline epitaxial layer technologies that were disclosed to Tower through the specific named inventors on the patents and patent application in question, who are its agents. These named inventors are Paul D. Hurwitz, Edward Preisler, David Howard, and Marco Racanelli.

106. Throughout their negotiations, Tower repeatedly and explicitly showed particular interest in obtaining exclusive access to RF applications of IQE's porous silicon and crystalline epitaxial wafers, products that Tower did not manufacture. Specifically, Tower wanted exclusivity for porous RF switches (the subject matter later claimed in the '740 patent and '712 application) and localized patterning of porous regions (the subject matter later claimed in the '920 patent).

107. During the period in which Tower was applying for the patents and immediately preceding this timeframe, in response to Tower's requests and in good faith, IQE provided the named inventors with technical information, experimental

data, explanations of various features of the technology, as well as answered questions from the named inventors.

108. Richard Hammond, Rodney Pelzel, and Andrew Clark have each been employees of IQE since 2016 or earlier and had previously assigned all right and title to their inventions and work to IQE.

109. Tower's sudden patenting of the same technology they were attempting to negotiate an exclusive access deal for was not independent of Richard Hammond, Rodney Pelzel, and Andrew Clark's work, as the patents were derived from the information provided to them by Richard Hammond, Rodney Pelzel, and Andrew Clark through the open line of communication by which the parties discussed their ongoing business relationship.

110. On information and belief, Tower did not and does not have any independent research capabilities regarding porous Si technology and was not aware of the technical features of IQE's porous Si products and processes until that information was communicated to Tower through its NDA-protected meetings with IQE.

111. IQE's contributions to the '740, '920, and '572 patents, and '712 application amounted to the entire conception and reduction to practice of the inventions in question, including an epitaxial layer on porous silicon and incorporating a semiconductor device in the epitaxial layer. IQE provided the named inventors with far more than well-known principles, nor did Richard Hammond, Rodney Pelzel, and Andrew Clark merely explain the state of the art. When measured against the full inventions, Richard Hammond, Rodney Pelzel, and Andrew Clark's work contributed substantially to both the conception and reduction to practice of the inventions claimed in all three patents and the patent application.

112. Neither Richard Hammond, Rodney Pelzel, or Andrew Clark, nor any other member of IQE is listed on any of the patents or patent applications as an inventor. Furthermore, the patents are solely assigned to Newport Fab, LLC.

113. The first of these patents was applied for on October 9, 2019, and was published on April 15, 2021. Before April 2021, there was no reasonable diligence which could have uncovered Tower's wrongdoing, thus April 2021 should be considered the date of discovery.

114. Thus this action has been brought before six years have passed since IQE knew or reasonably should have known of Tower's wrongdoing, and Tower is not entitled to a presumption of laches.

115. IQE's and IQE's employees' absence from the patents in question was not due to any deceptive intent on the part of IQE or its employees.

116. Due to the substantial contributions by Richard Hammond, Rodney Pelzel, and Andrew Clark upon which Paul Hurwitz, Edward Preisler, David Howard, and Marco Racanelli depended, IQE is entitled to a correction of inventorship to include (1) add Richard Hammond, Rodney Pelzel, and Andrew Clark and (2) remove the currently named inventors.

117. Further, IQE is entitled to injunctive relief in the form of an order for Tower to cease and desist from practicing the patents in question, and from further use of the misappropriated trade secrets when pursuing patents in the future.

COUNT IV:

Breach of Contract

118. IQE incorporates by reference each and every allegation contained in paragraphs 1–117 above as if fully set forth herein.

119. Among other agreements, IQE signed a mutually binding Non-Disclosure Agreement effective November 12, 2015, with Tower, which also bound its affiliates such as Newport Fab, LLC (then Jazz Semiconductor Inc). *See* Exhibit 1.

120. This NDA imposed a duty on both parties to protect any "Confidential Information" which is defined in the NDA to include "all information, documents, data, reports, interpretations, forecast, analyses, compilations, studies, ideas,

inventions (whether or not patentable), trade secrets and works of authorship, proprietary information, or records of or concerning the disclosing party or its affiliates, provided by the Disclosing Party to the receiving party," for a period of at least five years from the date of disclosure. *Id.*

121. During their negotiations, and beginning on November 6, 2018, IQE disclosed Confidential Information relating to their trade secrets and to their porous silicon wafers in particular.

122. By using and disclosing this information to pursue a patent on porous silicon semiconductors, Tower breached its contractual duty with IQE.

123. Therefore, IQE is entitled to damages and injunctive relief due to Tower's breach of the NDA.

COUNT V:

Violation of California Unfair Competition Law (Cal. Bus. And Professions Code § 17200)

124. IQE incorporates by reference each and every allegation contained in paragraphs 1–123 above as if fully set forth herein.

125. On a date that is currently unknown, but while the negotiations with IQE were still ongoing, Tower began a course of conduct consisting of actions of unfair competition as defined by California Business and Professions Code § 17200, by engaging in the practices herein described, including filing multiple patent applications with the USPTO disclosing and claiming IQE's trade secret and proprietary technology.

126. Tower's acts violate the California Business and Professions Code § 17200 in that Tower misappropriated and misused IQE's proprietary information and intellectual property, fraudulently negotiated with IQE to gain access to their trade secrets, and used IQE's proprietary information for their own benefit and without the consent of IQE.

127. The harm to IQE, IQE's customers, and the public at large outweighs any potential utility of Tower's conduct.

128. Tower's actions herein described constitute unlawful, unfair, and fraudulent business practices within the meaning of California Business Code § 17200, which pose a threat, and will continue to pose a threat to IQE and to IQE's customers.

129. As a direct result of the aforementioned acts, IQE is entitled to injunctive relief as may be necessary to prevent the use or employment of said unfair business practices, and an order of restitution compelling Tower to disgorge the profits which resulted from their wrongdoing.

COUNT VI:

Intentional Interference with Prospective Economic Advantage

130. IQE incorporates by reference each and every allegation contained in paragraphs 1–129 above as if fully set forth herein.

131. IQE has developed numerous business and contractual relationships with existing and potential customers, based on their ability to provide unique and custom semiconductor solutions by using their proprietary systems and technology. These relationships carried with them the probability of future economic benefit to IQE.

132. Tower has, and at all relevant times herein alleged had, knowledge of the existence of IQE's business and contractual relations. Indeed, a sticking point of negotiations between IQE and Tower is that IQE planned and worked to continue to solicit these potential customers and thus rejected Tower's request for an exclusive arrangement.

133. In the past, Tower sought to secure an advantageous market system by entering into an exclusive contract with IQE, in order to benefit from IQE's trade secrets. Indeed, Tower insisted on exclusivity as essential to any supplier agreement.

134. Had Tower been the true inventor of the technology now claimed in its patents, it would not have needed exclusivity through contract. There is no reason to insist on contractual exclusivity where exclusive rights are secured through patents. Tower's behavior confirms that it did not believe itself to have exclusive rights to IQE's porous silicon technology.

135. Having been denied an exclusive deal with IQE, Tower now seeks to gain by deception what it could not gain through negotiation. By using patent rights to gain exclusive rights to IQE's trade secrets, Tower looks to force IQE's hand, compelling it to deal with Tower—and Tower alone—in order to practice its own technology.

136. Furthermore, a core of IQE's business is the development of unique and custom semiconductor solutions for customers. For that reason, customers not only engage IQE based on their current portfolio of solutions but also on the basis of prospective technologies that IQE can develop. The existence of these patents disrupts IQE's ability to innovate compound semiconductors integrating porous silicon, and other prospective solutions that use porous silicon and crystalline epitaxy, substantially disrupting IQE's market position and trajectory.

137. Beyond the patents and patent application in question, the unlawful disclosures of IQE's trade secrets alone disrupts IQE's business relations with current and prospective customers by enabling others to compete with IQE using the trade secret information disclosed in the patents to replicate IQE's products. Additionally, the threat of enforcement of Tower's patents against IQE or its customers undermines IQE's ability to freely offer its technology in the marketplace.

138. As a proximate result of Tower's interference with IQE's prospective economic advantage, IQE's customer relationships have been disrupted. IQE's ability to compete in the marketplace for porous silicon has been damaged. IQE is

entitled to recover compensatory damages in an amount exceeding the minimum jurisdictional limit of this Court and subject to proof at trial.

139. Tower's acts were willful and malicious insofar as Defendants committed such acts with the intent to injure IQE's business, and to increase their own profits with conscious disregard for IQE's rights, thereby warranting an award of punitive damages in an amount sufficient to punish Tower and deter others from engaging in similar misconduct.

COUNT VII:

Negligent Interference with Prospective Economic Advantage

140. IQE incorporates by reference each and every allegation contained in paragraphs 1–139 above as if fully set forth herein.

141. In engaging in the conduct and actions described herein, Tower also negligently interfered with IQE's existing business relationships with customers and undermined or interfered with the acquisition of new customers, all of which carried the probability of future economic benefit to IQE.

142. As a proximate result of the wrongful acts herein alleged, IQE has been damaged in an amount exceeding the minimum jurisdictional limit of this Court and subject to proof at trial.

PRAYER FOR RELIEF

WHEREFORE, IQE prays for judgment against Tower as follows:

1. For injunctive relief in the form of a correction of inventorship of the U.S. Patent Nos. 11,164,740, 11,195,920, and 11,145,572 and U.S. Patent Application 17/400,712;

2. For compensatory damages in a sum according to proof;

3. For the statutory remedies specified in the Defend Trade Secrets Act and the California Uniform Trade Secrets Act, including the recovery of an amount equal to Tower's unjust enrichment and any reasonable royalties the Court deems necessary and appropriate;

4. For punitive damages in a sum according to proof;

5. For the contractual damages for breach of the parties' NDA;

6. For an award of attorney's fees as permitted under the Defend Trade Secrets Act and the California Uniform Trade Secrets Act;

7. For interest at the legal rate;

8. For an order enjoining Tower and their agents, servants, employees, employers, and all persons acting under, in concert with, of or for them from further using or soliciting customers based on their wrongful possession of IQE's trade secrets;

9. For an order declaring that Tower and their agents, servants, employees, employers, and all persons acting under, in concert with, of or for them, are preliminarily and permanently enjoined from acts constituting a violation of the Defend Trade Secrets Act, the California Uniform Trade Secrets Act, and the California Unfair Competition Statute, including the misappropriation of trade secrets, pursuant to 18 U.S.C § 1836(b)(3)(A), CA Civ. Code § 3246.5, and the equitable powers of the Court;

10. For the costs incurred in this action; and

11. For such other and further relief as the Court deems just and proper.

Dated: April 27, 2022

/s/ Karin G. Pagnanelli

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JURY DEMAND

IQE demands a trial by jury on all matters alleged herein in accordance with the Seventh Amendment to the U.S. Constitution and Rule 38(b) of the Federal Rules for Civil Procedure.

Dated: April 27, 2022

/s/ Karin G. Pagnanelli

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Exhibit 1

TOWERJAZZ

Non-Disclosure Agreement

Effective Date: 11th November 12, 2015.

In order to protect certain confidential information, **Tower Semiconductor Ltd.** whose principal address is Ramat Gavriel Industrial Park, P.O. Box 619 Migdal Haemek 23105, Israel and its affiliates, including **Jazz Semiconductor, Inc.** whose principal address is 4321 Jamboree Road, Newport Beach, CA 92660, USA and **TowerJazz Panasonic Semiconductor Co., Ltd.** whose principal address is 800 Higashiyama, Uozu City, Toyama 937-8585, Japan (collectively, "TowerJazz") as one party, and IQE plc, , whose principal address is Pascal Close, St Mellons, Cardiff, Wales, UK CF3 0LW (the "Customer") as the other party, hereby enter into this Non-Disclosure Agreement ("Agreement") and agree that:

1. "Confidential Information" (also referred to as "CI") means all information, documents, data, reports, interpretations, forecasts, analyses, compilations, studies, ideas, inventions (whether or not patentable), trade secrets and works of authorship, proprietary information, or records of or concerning the disclosing party or its affiliates (the "Disclosing Party"), provided by the Disclosing Party to the receiving party (the "Recipient"), as well as all information in tangible form that bears a "confidential," "proprietary," "secret," or similar legend, and discussions relating to that information whether those discussions occur prior to, concurrent with, or following disclosure of the information. The Disclosing Party shall make reasonable efforts to mark its Confidential Information in tangible form with any of the aforementioned legends prior to disclosure. However, the Disclosing Party's information in tangible form that does not bear any of these legends, and discussions relating to that information, shall nevertheless be protected hereunder as Confidential Information, if the Recipient knew, or should have reasonably known under the circumstances, that the information is confidential or if such information had been communicated in confidence. Confidential Information shall also include, without limitation, all information obtained by Recipient from any website hosted by or on behalf of the Disclosing Party that is not accessible to the general public but is accessible via a password and user name.

2. The Recipient shall not disclose CI to any third party (except as provided herein below) and shall make use of CI only for wafer manufacturing at TowerJazz, including related processes and services (the "Purpose").

3. The Recipient's duties hereunder expire 5 years from the date of disclosure. However, subject to section 5 below, the confidentiality obligation to protect TowerJazz's design kits (including design rules, EDA and PDK documentations and run sets) shall not expire.

4. Recipient shall protect the disclosed CI from any unauthorized use, dissemination or publication using the same degree of care Recipient uses to protect its own information of a like nature and sensitivity, but no less than a reasonable degree of care. Recipient will not disclose any of the Disclosing Party's CI, except to its employees, bankers, accountants, attorneys, consultants or subcontractors who have a need to know for the Purpose and who agree to abide by nondisclosure terms at least as comprehensive as those set forth herein.

5. This Agreement imposes no obligation upon Recipient to the extent any CI (a) was rightfully in Recipient's possession before receipt thereof under this Agreement; (b) is generally available to the public at the time of disclosure or becomes public knowledge through no fault of Recipient; (c) is rightfully received by Recipient from a third party without a duty of confidentiality; or (d) was independently developed by Recipient without use of the Confidential Information received from the Disclosing Party, as evidenced in writing. Recipient may disclose CI to the extent required by any law, regulation or other applicable judicial or governmental order. Unless legally prohibited, Recipient will timely notify the Disclosing Party of such disclosure requirement in advance of the required disclosure so as to allow the Disclosing Party the opportunity to oppose or limit such disclosure.

6. Each Disclosing Party warrants that it has the right to make the disclosures made under this Agreement. NO OTHER WARRANTIES ARE MADE BY EITHER PARTY UNDER THIS AGREEMENT. ANY INFORMATION EXCHANGED UNDER THIS AGREEMENT IS PROVIDED "AS IS".

7. Neither party acquires any intellectual property rights under this Agreement. The CI of Disclosing Party shall remain the property of the Disclosing Party, and shall be returned to the Disclosing Party promptly upon written request, or destroyed at the Disclosing Party's option. Recipient agrees to promptly provide written confirmation to Disclosing Party of its compliance with any such request.

8. This Agreement imposes no obligations on either party to purchase, sell, license, transfer or otherwise dispose of any technology, service or products or enter into any other business relationship with the other party.

9. The Recipient acknowledges its obligations to control access to technical data under the U.S. Export Administration laws and regulations and/or other applicable local regulations and agrees to adhere to such laws and regulations with regard to any CI received under this Agreement. Recipient will not export outside the United States, if a United States company or citizen, or re-export, if a foreign company or citizen, except as permitted by said laws and regulations.

CUSTOMER HEREBY DECLARES THAT THE CONFIDENTIAL INFORMATION (CHECK ONE):

X Is not intended to design product(s) for use with, derived from, or developed specifically for a military application or any radiation hardened or space application, or for use in any such item.

☐ Is intended to design product(s) for use with, derived from, or developed specifically for military application or any radiation hardened or space application, or for use in any such item.

10. It is understood and agreed that the unauthorized use or disclosure of any CI may cause irreparable harm to the Disclosing Party. Accordingly, Recipient agrees that the Disclosing Party will have the right to seek an immediate injunction against any breach or threatened breach of this Agreement without the need for proof of actual damages, as well as the right to pursue any and all other rights and remedies available at law or in equity for such a breach.

11. No failure or delay in exercising any right, power or privilege hereunder shall operate as a waiver thereof, nor shall any single or partial exercise thereof preclude any future exercise thereof or any exercise thereof under applicable law or in equity. This Agreement is the entire and only agreement between the parties hereto with respect to its subject matter, and supersedes all prior and contemporaneous understandings, discussions and agreements with respect to such subject matter. All additions or modifications to this Agreement must be made in writing and agreed to by both parties. This Agreement may be executed in counterparts. This Agreement may not be assigned by either party without the other party's prior written consent.

12. This Agreement, as well as any disputes arising out of or relating to this Agreement, shall be interpreted under and governed by the laws of the State of California. Any disputes arising out of or relating to this Agreement and not resolved by the parties themselves shall be commenced solely in the federal or state courts located within the State of California. In such event, each party irrevocably agrees to submit to the personal jurisdiction of such courts and irrevocably waives any objection to such venue. The parties agree that the State of California has a reasonable relationship to the subject matter of this Agreement and that there is a reasonable basis for the selections of governing law and venue set forth above.

TowerJazz

Signature: [signature]

By: Zmira Luvic
Title: GM TOPS BU

Company: IQE plc.

Signature: [signature]

By: Drew Nelson
Title: President /CEO.

MW

Exhibit 2

US011164740B2

(12) **United States Patent**
Hurwitz et al.

(10) **Patent No.: US 11,164,740 B2**
(45) **Date of Patent: Nov. 2, 2021**

(54) **SEMICONDUCTOR STRUCTURE HAVING POROUS SEMICONDUCTOR LAYER FOR RF DEVICES**

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(73) Assignee: **Newport Fab, LLC**, Newport Beach, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **16/597,779**

(22) Filed: **Oct. 9, 2019**

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(51) **Int. Cl.**

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H01L 29/04	(2006.01)
H01L 29/08	(2006.01)
H01L 23/66	(2006.01)
H03K 17/687	(2006.01)
H01L 21/762	(2006.01)

(52) **U.S. Cl.**

CPC .. ***H01L 21/02203*** (2013.01); ***H01L 21/76294*** (2013.01); ***H01L 23/66*** (2013.01); ***H01L 29/04*** (2013.01); ***H01L 29/0843*** (2013.01); ***H03K 17/687*** (2013.01); *H01L 2223/6677* (2013.01)

(58) **Field of Classification Search**

CPC H01L 21/02203; H01L 21/76294; H01L 29/04; H01L 29/0843; H01L 23/66; H01L 17/687; H01L 27/687; H01L 2223/6677; H01L 21/02; H01L 29/08; H01L 21/762; H03K 17/687

USPC 257/728

See application file for complete search history.

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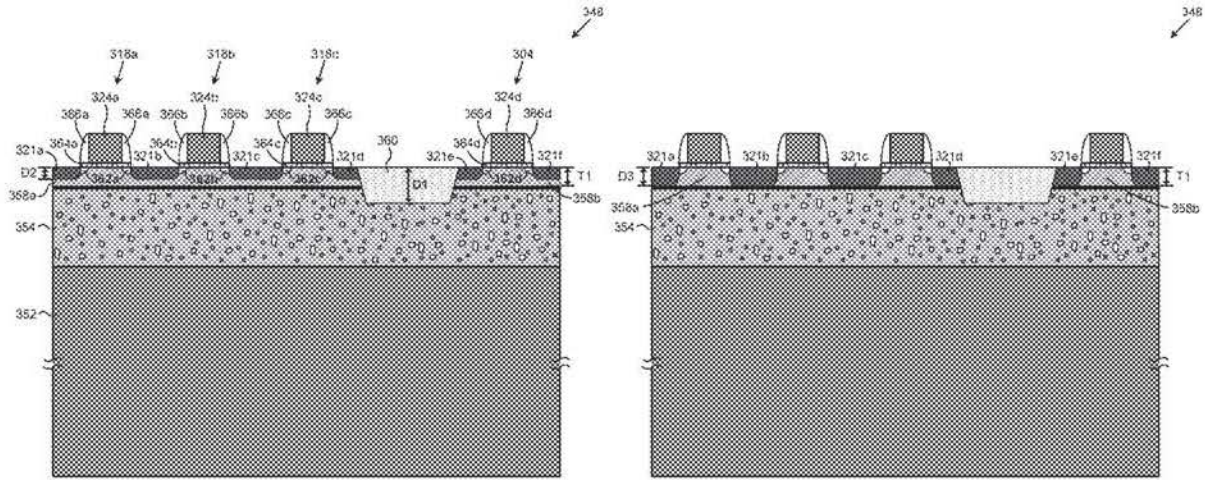
Primary Examiner — Alexander O Williams

(74) *Attorney, Agent, or Firm* — Farjami & Farjami LLP

(57) **ABSTRACT**

A semiconductor structure includes a substrate having a first dielectric constant, a porous semiconductor layer situated over the substrate, and a crystalline epitaxial layer situated over the porous semiconductor layer. A first semiconductor device is situated in the crystalline epitaxial layer. The porous semiconductor layer has a second dielectric constant that is substantially less than the first dielectric constant such that the porous semiconductor layer reduces signal leakage from the first semiconductor device. The semiconductor structure can include a second semiconductor device situated in the crystalline epitaxial layer, and an electrical isolation region separating the first and second semiconductor devices.

20 Claims, 8 Drawing Sheets



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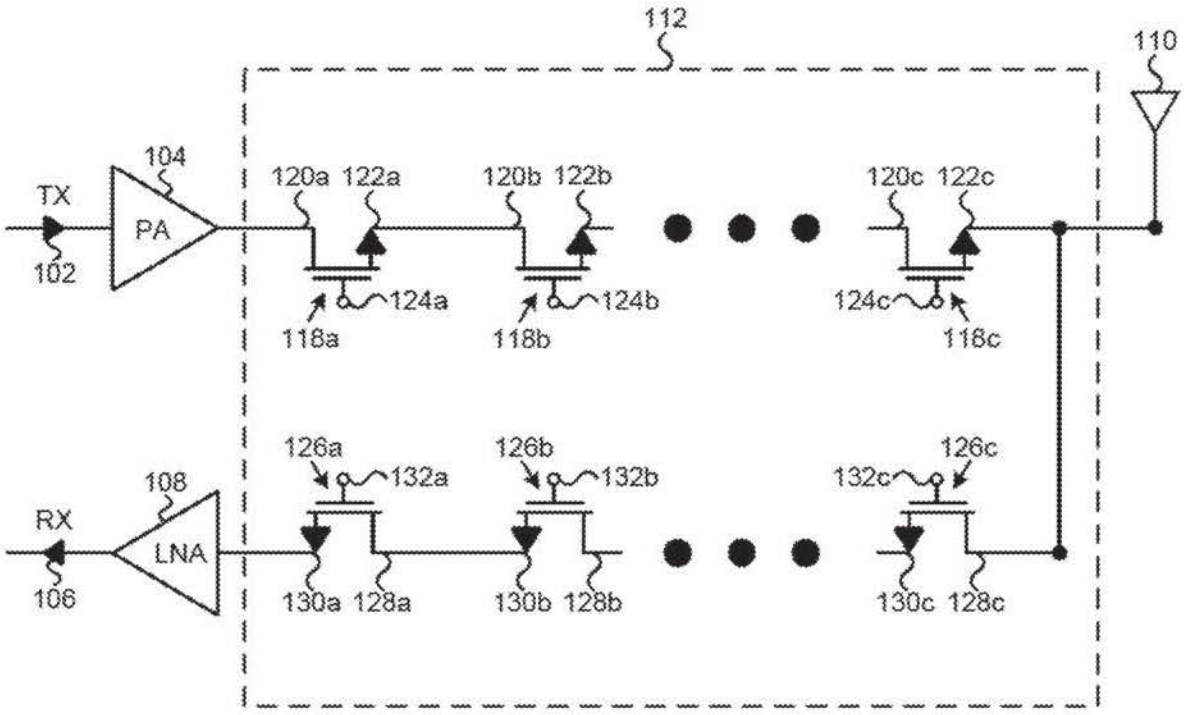
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110
104
TX
PA
102
120a 122a
120b 122b
120c 122c
124a
124b
124c
118a
118b
118c
126a
126b
126c
132a
132b
132c
108
RX
LNA
106
130a 128a
130b 128b
130c 128c

FIG. 1

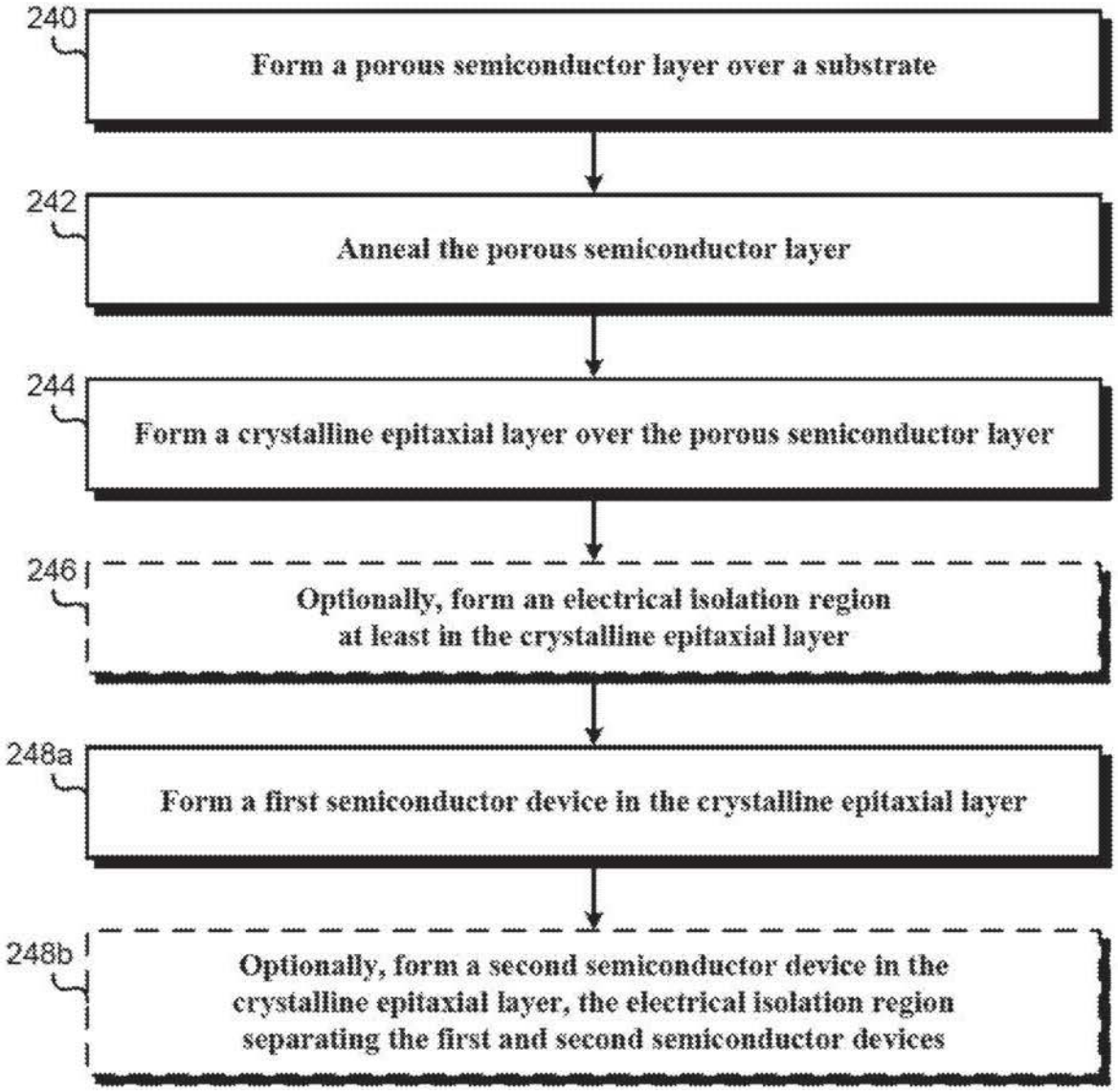

240
Form a porous semiconductor layer over a substrate
242
Anneal the porous semiconductor layer
244
Form a crystalline epitaxial layer over the porous semiconductor layer
246
Optionally, form an electrical isolation region at least in the crystalline epitaxial layer
248a
Form a first semiconductor device in the crystalline epitaxial layer
248b
Optionally, form a second semiconductor device in the crystalline epitaxial layer, the electrical isolation region separating the first and second semiconductor devices

FIG. 2

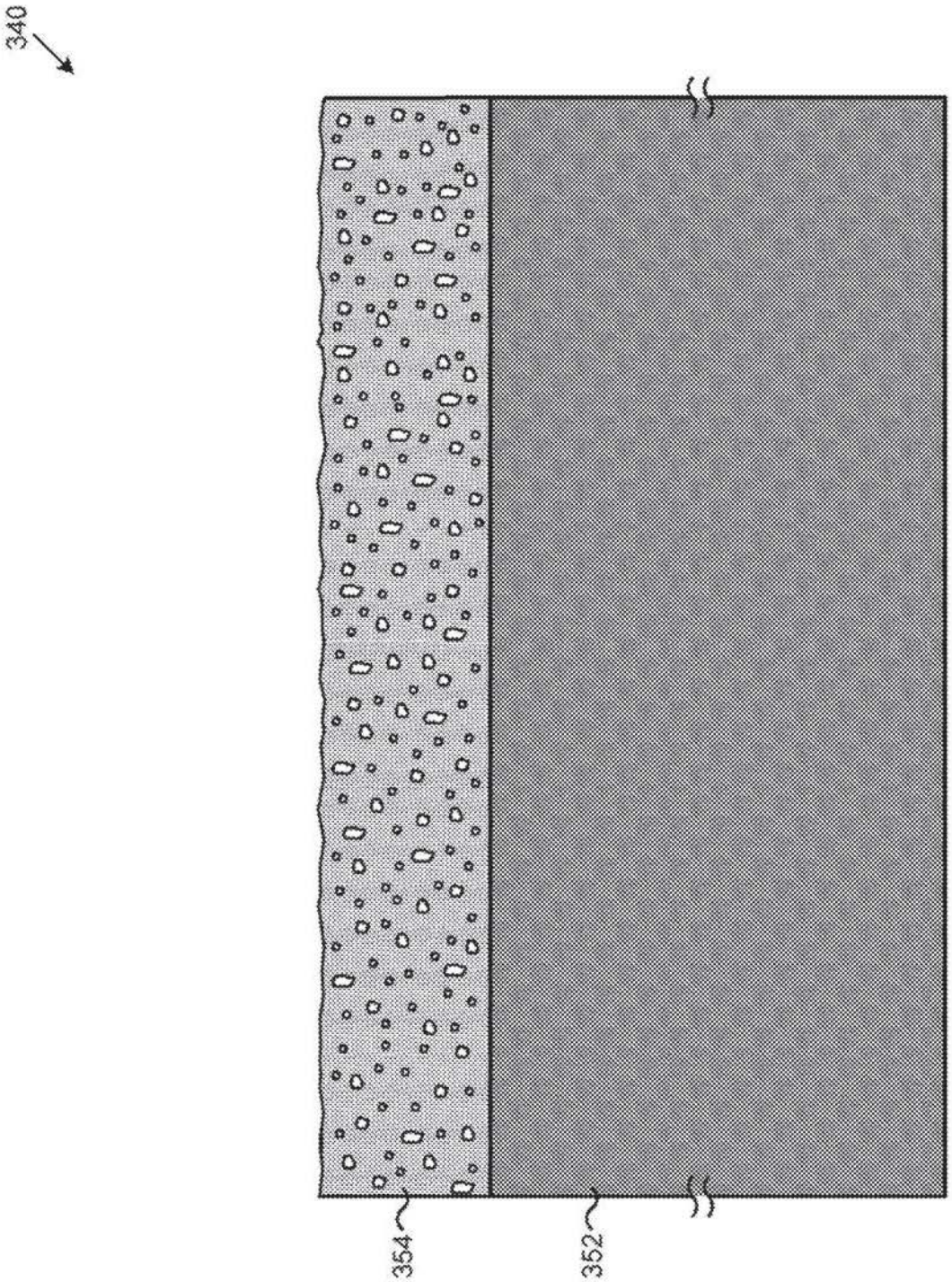


FIG. 3A

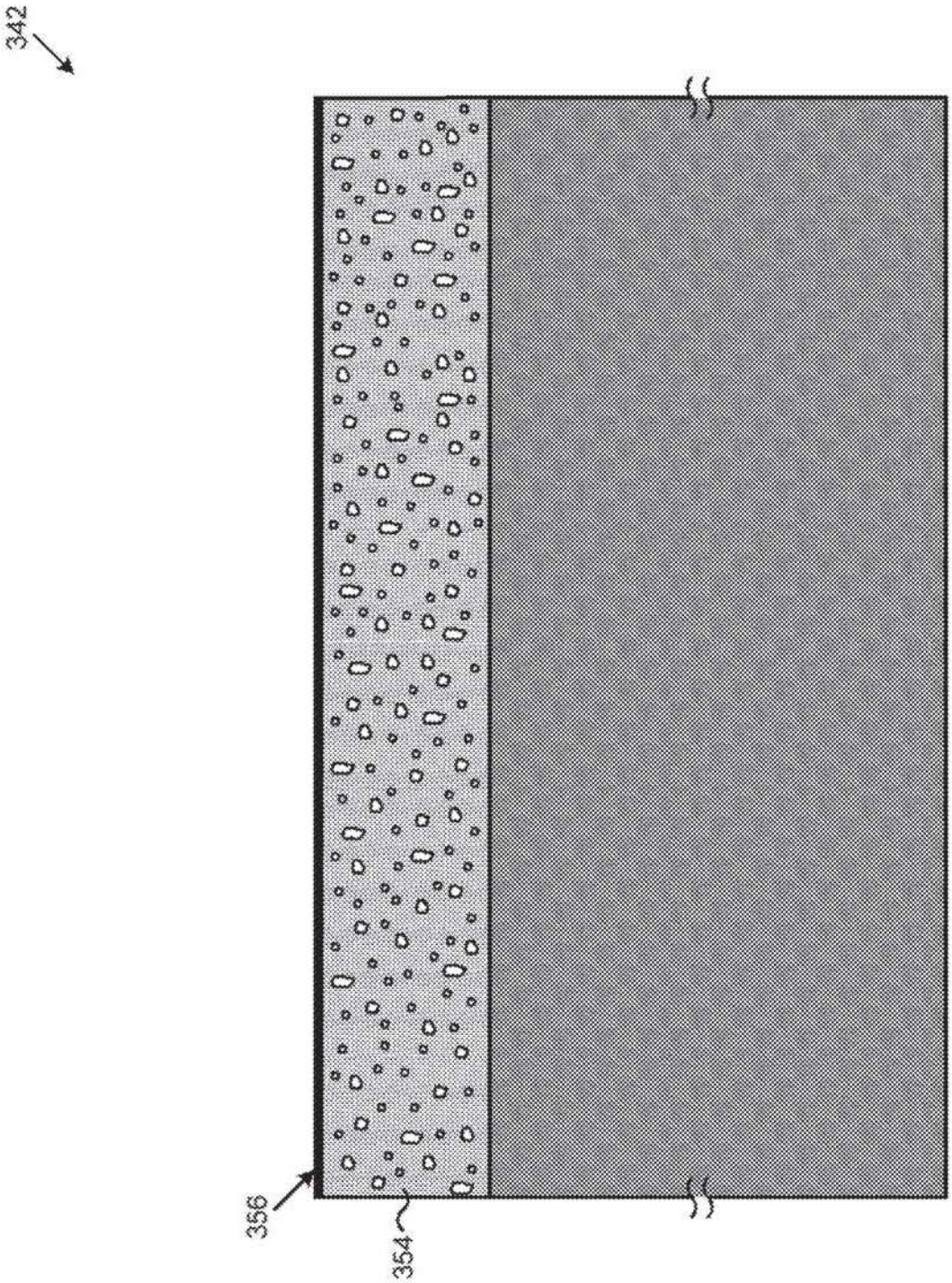


FIG. 3B

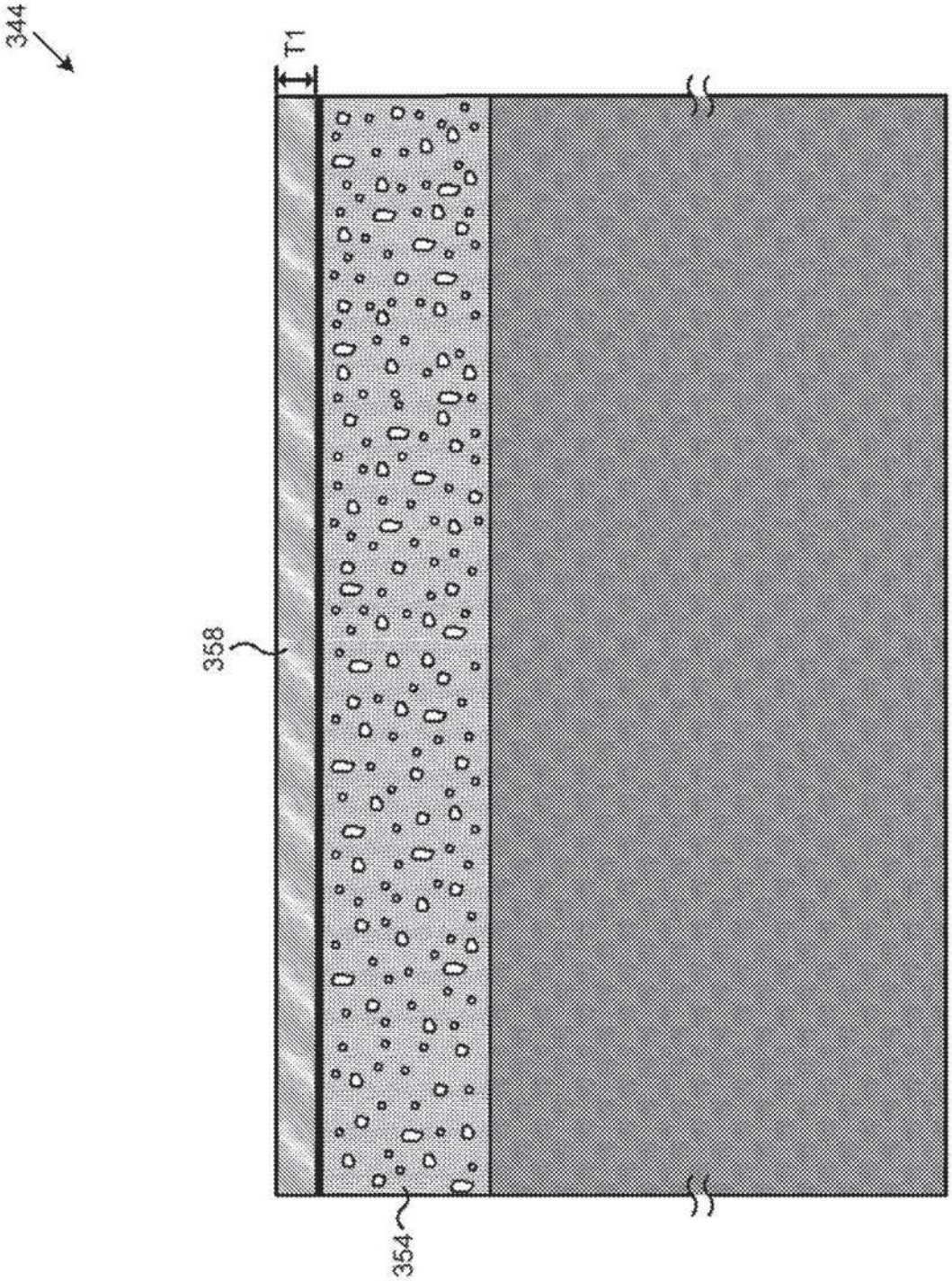


FIG. 3C

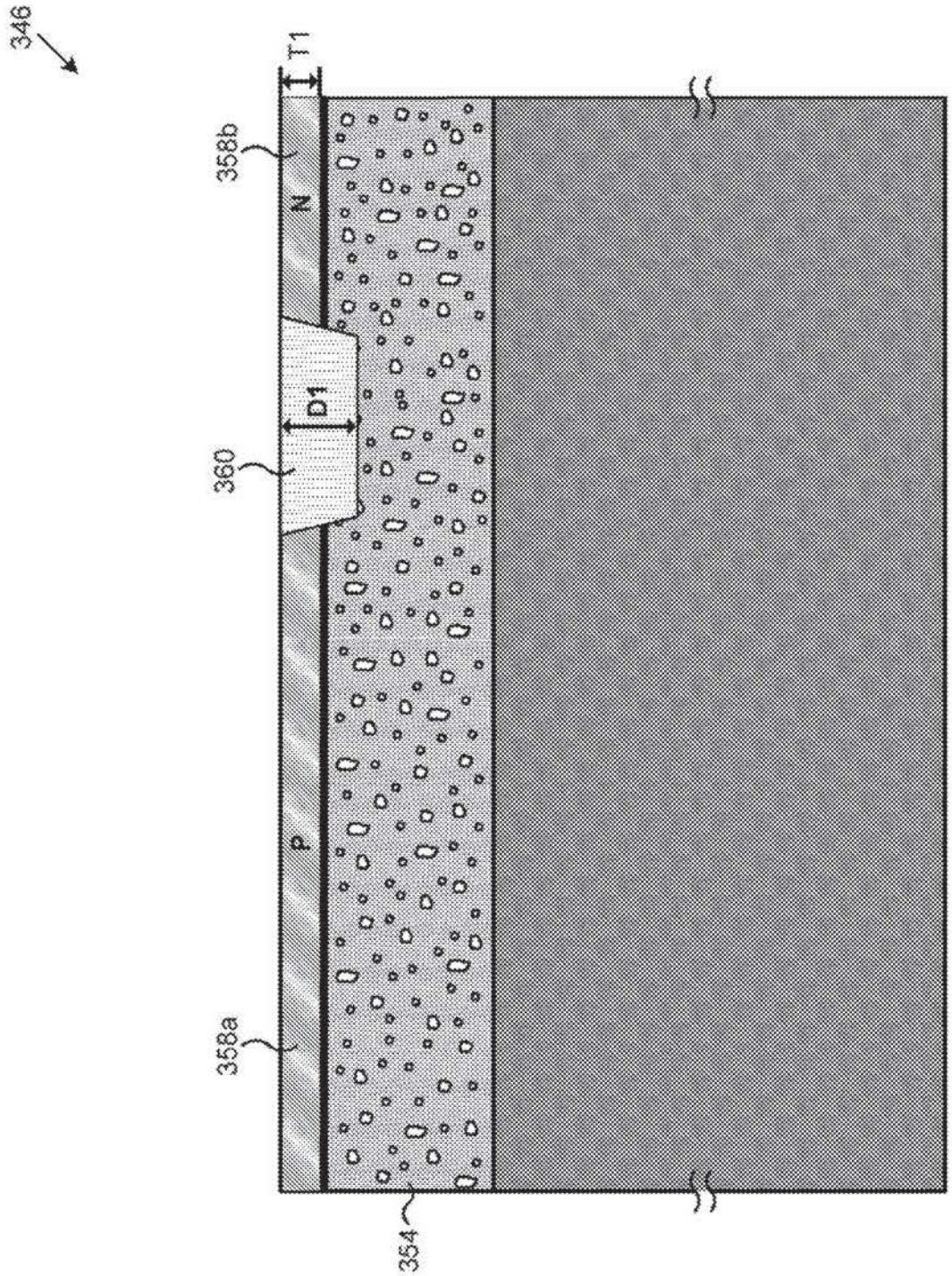
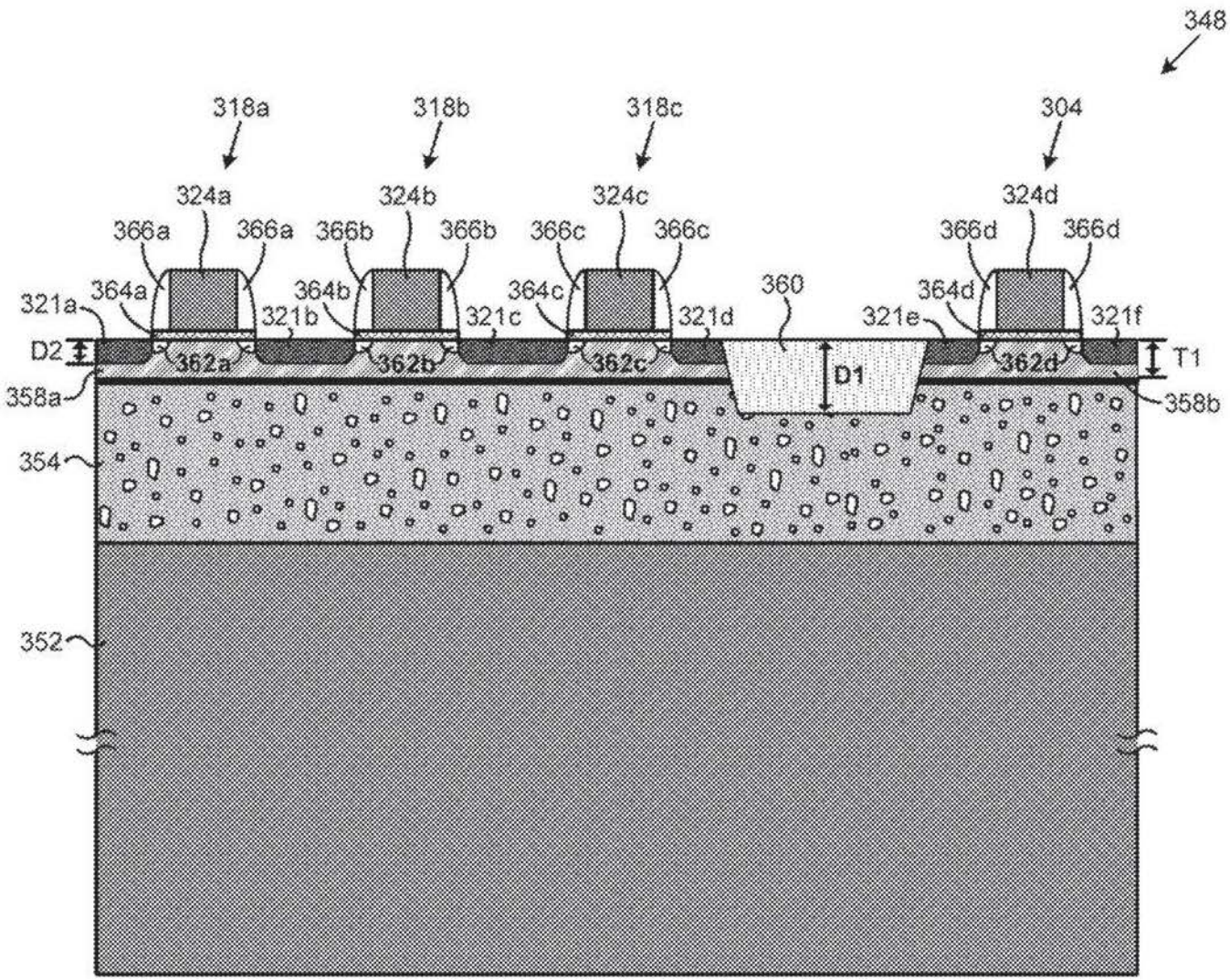


FIG. 3D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318b
318c
304
324a
324b
324c
324d
366a
366a
366b
366b
366c
366c
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321a
364a
364b
321b
321c
364c
360
321d
364d
321e
321f
D2
362a
362b
362c
D1
362d
T1
358a
358b
354
352

FIG. 3E

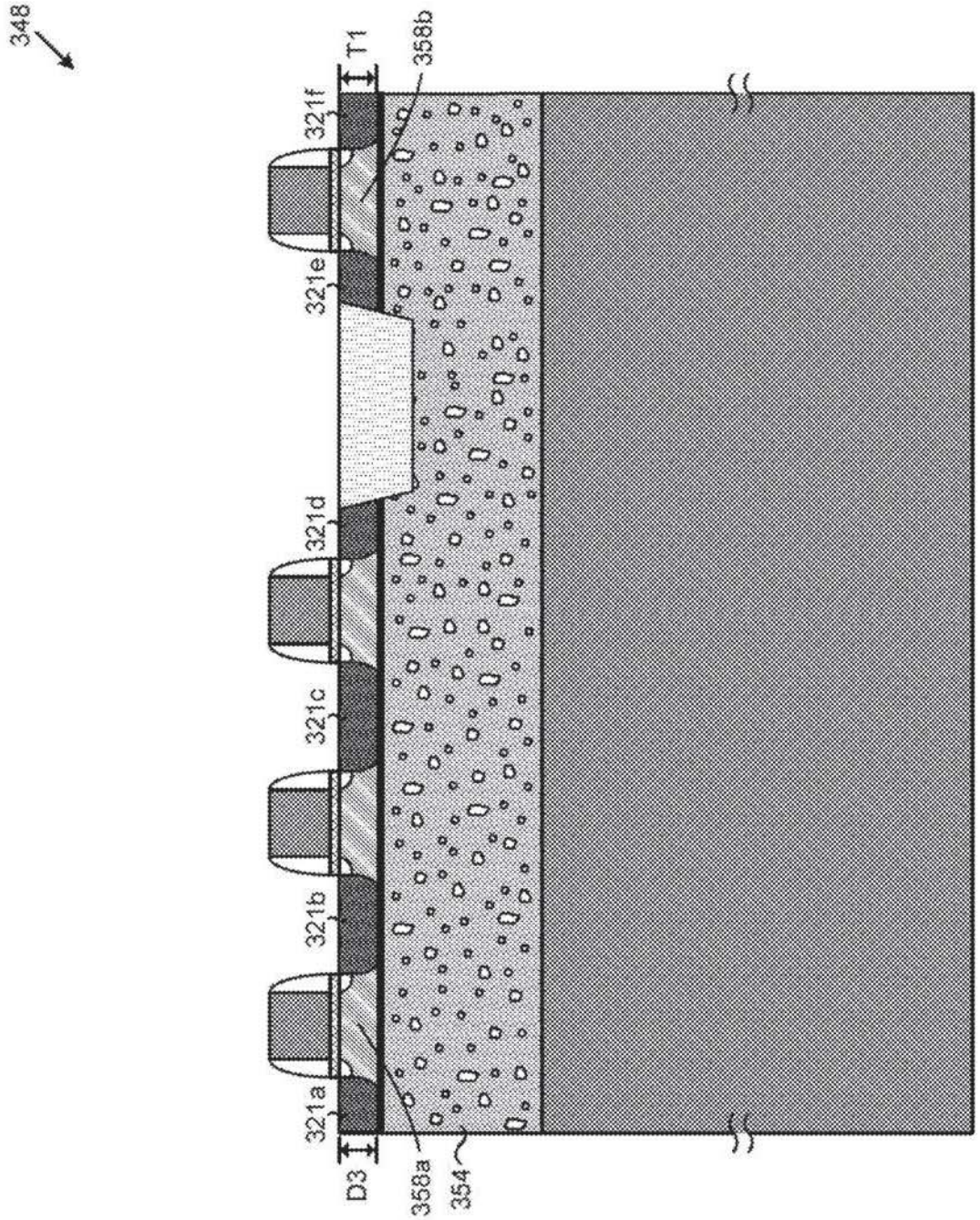

FIG. 3F

SEMICONDUCTOR STRUCTURE HAVING POROUS SEMICONDUCTOR LAYER FOR RF DEVICES

BACKGROUND

Semiconductor-on-insulator (SOI) structures are commonly employed to realize radio frequency (RF) designs where low signal leakage is required. These SOI structures use a buried oxide (BOX) under a top device layer in which RF circuit components, such as transistors and/or passive components, are fabricated.

As known in the art, a handle wafer finctioning as a substrate under the BOX results in some signal leakage. In one approach, a high resistivity silicon is used for the handle wafer in order to improve isolation and reduce signal loss. However, the relatively high dielectric constant of silicon (k=11.7) results in significant capacitive loading of RF SOI devices. In another approach, a trap-rich layer is formed between the handle wafer and the BOX in order to minimize parasitic surface conduction effects that would adversely affect RF devices in the top device layer. However, this approach requires costly and/or specialized fabrication techniques.

Thus, there is need in the art for efficiently and effectively fabricating RF devices with reduced signal leakage at low cost while overcoming the disadvantages and deficiencies of the previously known approaches.

SUMMARY

The present disclosure is directed to a semiconductor structure having porous semiconductor layer for RF devices, substantially as shown in and/or described in connection with at least one of the figures, and as set forth in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates a portion of a transceiver including a radio frequency (RF) switch employing stacked transistors according to one implementation of the present application.

FIG. **2** illustrates a portion of a flowchart of an exemplary method for manufacturing a semiconductor structure according to one implementation of the present application.

FIG. **3**A illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **240** in the flowchart of FIG. **2** according to one implementation of the present application.

FIG. **3**B illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **242** in the flowchart of FIG. **2** according to one implementation of the present application

FIG. **3**C illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **244** in the flowchart of FIG. **2** according to one implementation of the present application

FIG. **3**D illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **246** in the flowchart of FIG. **2** according to one implementation of the present application.

FIG. **3**E illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with actions **248***a* and **248***b* in the flowchart of FIG. **2** according to one implementation of the present application.

FIG. **3**F illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with actions **248***a* and **248***b* in the flowchart of FIG. **2** according to one implementation of the present application.

DETAILED DESCRIPTION

The following description contains specific information pertaining to implementations in the present disclosure. The drawings in the present application and their accompanying detailed description are directed to merely exemplary implementations. Unless noted otherwise, like or corresponding elements among the figures may be indicated by like or corresponding reference numerals. Moreover, the drawings and illustrations in the present application are generally not to scale, and are not intended to correspond to actual relative dimensions.

FIG. **1** illustrates a portion of a transceiver including a radio frequency (RF) switch employing stacked transistors according to one implementation of the present application. The transceiver in FIG. **1** includes transmit input **102**, power amplifier (PA) **104**, receive output **106**, low-noise amplifier (LNA) **108**, antenna **110**, and radio frequency (RF) switch **112**.

RF switch **112** is situated between PA **104** and antenna **110**. PA **104** amplifies RF signals transmitted from transmit input **102**. In one implementation, transmit input **102** can be coupled to a mixer (not shown in FIG. **1**), or to another input source. The output of PA **104** is coupled to one end of RF switch **112**. A matching network (not shown in FIG. **1**) can be coupled between PA **104** and RF switch **112**. Another end of RF switch **112** is coupled to antenna **110**. Antenna **110** can transmit amplified RF signals. In one implementation, RF switch **112** can be coupled to an antenna array, rather than a single antenna **110**.

RF switch **112** is also situated between LNA **108** and antenna **110**. Antenna **110** also receives RF signals. Antenna **110** is coupled to one end of RF switch **112**. Another end of RF switch **112** is coupled to the input of LNA **108**. LNA **108** amplifies RF signals received from RF switch **112**. A matching network (not shown in FIG. **1**) can be coupled between RF switch **112** and LNA **108**. Receive output **106** receives amplified RF signals from LNA **108**. In one implementation, receive output **106** can be coupled to a mixer (not shown in FIG. **1**), or to another output source.

RF switch **112** includes two stacks of transistors. The first stack includes transistors **118***a*, **118***b*, and **118***c*. Drain **120***a* of transistor **118***a* is coupled to the output of PA **104**. Source **122***a* of transistor **118***a* is coupled to drain **120***b* of transistor **118***b*. Source **122***b* of transistor **118***b* can be coupled to the drain of additional transistors, and ultimately coupled to drain **120***c* of transistor **118***c*. Source **122***c* of transistor **118***c* is coupled to antenna **110**. Gates **124***a*, **124***b*, and **124***c* of transistors **118***a*, **118***b*, and **118***c* respectively can be coupled to a controller or a pulse generator (not shown) for switching transistors **118***a*, **118***b*, and **118***c* between ON and OFF states.

The second stack includes transistors **126***a*, **126***b*, and **126***c*. Source **130***a* of transistor **126***a* is coupled to the input of LNA **108**. Drain **128***a* of transistor **126***a* is coupled to source **130***b* of transistor **126***b*. Drain **128***b* of transistor **126***b* can be coupled to the drain of additional transistors, and ultimately coupled to drain source **130***c* of transistor **126***c*. Drain **128***c* of transistor **126***c* is coupled to antenna **110**. Gates **132***a*, **132***b*, and **132***c* of transistors **126***a*, **126***b*, and **126***c* respectively can be coupled to a controller or a pulse generator (not shown) for switching transistors **126***a*, **126***b*, and **126***c* between ON and OFF states.

In the example of FIG. **1**, RF switch **112** switches the transceiver in FIG. **1** between receive and transmit modes. When transistors **118***a*, **118***b*, and **118***c* are in OFF states, and transistors **126***a*, **126***b*, and **126***c* are in ON states, the transceiver is in receive mode. Transistors **126***a*, **126***b*, and **126***c* serve as a receive path for RF signals received by antenna **110** to pass to LNA **108** and to receive output **106**. When transistors **118***a*, **118***b*, and **118***c* are in ON states, and transistors **126***a*, **126***b*, and **126***c* are in OFF states, the transceiver is in transmit mode. Transistors **118***a*, **118***b*, and **118***c* serve as a transmit path for RF signals transmitted from transmit input **102** and PA **104** to pass to antenna **110**. In various implementations, RF switch **112** can include more stacks of transistors and/or more amplifiers. In various implementations, RF switch **112** can switch the transceiver between two transmit modes corresponding to different frequencies, or between two receive modes corresponding to different frequencies.

In the present implementation, transistors **118***a*, **118***b*, **1/8***c*, **126***a*, **126***b*, and **126***c* are N-type field effect transistors (NFETs). In various implementations, transistors **118***a*, **118***b*, **118***c*, **126***a*, **126***b*, and **126***c* can be P-type FETs (PFETs), junction FETs (JFETs), or any other type of transistor. By stacking transistors **118***a*, **118***b*, **118***c*, **126***a*, **126***b*, and **126***c* as shown in FIG. **1**, the overall OFF state power and voltage handling capability for RF switch **112** can be increased. For example, if only transistors **118***a* and **126***a* were used, RF switch **112** may have an OFF state voltage handling capability of five volts (5 V). If eight transistors were used in each stack, RF switch **112** may have an OFF state voltage handling capability of forty volts (40 V). In various implementations. RF switch **112** can have more or fewer stacked transistors than shown in FIG. **1**.

As described below, in conventional semiconductor structures, signals can leak from RF switch **112**, for example, to ground or to other devices. This signal leakage is particularly problematic when transistors **118***a*, **118***b*, **118***c*, **126***a*, **126***b*, and **126***c* are in OFF states, and when dealing with higher frequency signals, such as RF signals. According to the present application, RF switch **112** can be utilized in a semiconductor structure that reduces signal leakage. It is noted that, although the present application focuses on RF signals, the signals may have frequencies other than RF frequencies.

FIG. **2** illustrates a portion of a flowchart of an exemplary method for manufacturing a semiconductor structure according to one implementation of the present application. Structures shown in FIGS. **3**A through **3**E illustrate the results of performing actions **240** through **248***b* shown in the flowchart of FIG. **2**. For example, FIG. **3**A shows a semiconductor structure after performing action **240** in FIG. **2**, FIG. **3**B shows a semiconductor structure after performing action **242** in FIG. **2**, and so forth.

Actions **240** through **248***b* shown in the flowchart of FIG. **2** are sufficient to describe one implementation of the present inventive concepts. Other implementations of the present inventive concepts may utilize actions different from those shown in the flowchart of FIG. **2**. Certain details and features have been left out of the flowchart of FIG. **2** that are apparent to a person of ordinary skill in the art. For example, an action may consist of one or more sub-actions or may involve specialized equipment or materials, as known in the art. Moreover, some actions, such as masking and cleaning actions, are omitted so as not to distract from the illustrated actions.

FIG. **3**A illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **240** in the flowchart of FIG. **2** according to one implementation of the present application. As shown in FIG. **3**A, according to action **240**, semiconductor structure **340** including porous semiconductor layer **354** situated over substrate **352** is formed. In the present implementation, substrate **352** is a bulk silicon substrate. For example, substrate **352** can be a P-type bulk silicon substrate having a thickness of approximately seven hundred microns (700 μm). In various implementations, substrate **352** may be any other type of substrate.

Porous semiconductor layer **354** situated over substrate **352** is a semiconductor layer having voids, or pores, therein. Within porous semiconductor layer **354**, the pores can have any orientation, branching, fill, or other morphological characteristic known in the art. Porous semiconductor layer **354** can be formed by using a top-down technique, where portions of substrate **352** are removed to generate pores. For example, porous semiconductor layer **354** can be formed by electrochemical etching using hydrofluoric acid (HF). Alternatively, porous semiconductor layer **354** can also be formed by stain etching, photoetching, or any other top-down technique known in the art. Porous semiconductor layer **354** can also be formed by using a bottom-up technique, where deposition results in a semiconductor layer having empty spaces. For example, porous semiconductor layer **354** can be formed by low-temperature high-density plasma (HDP) deposition. Alternatively, porous semiconductor layer **354** can also be formed by plasma hydrogenation of an amorphous layer, laser ablation, or any other bottom-up technique known in the art. In the present implementation, porous semiconductor layer **354** is a porous silicon layer, and has a thickness from approximately ten microns (10 μm) to approximately fifty microns (50 μm). In various implementations, porous semiconductor layer **354** may be any other type of porous semiconductor layer.

FIG. **3**B illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **242** in the flowchart of FIG. **2** according to one implementation of the present application. In semiconductor structure **342**, porous semiconductor layer **354** is annealed. For example, porous semiconductor layer **354** can be annealed in argon (Ar) or hydrogen (H_2) at atmospheric pressure from a temperature of approximately seven hundred degrees Celsius (700° C.) to a temperature of approximately eleven hundred degrees Celsius (1100° C.) for approximately ten minutes (10 min). Any other annealing technique known in the art can be utilized, such as techniques utilizing different temperatures, durations, and/or pressures. The annealing shown in FIG. **3**B reorganizes the pores in porous semiconductor layer **354** into larger cavities, while closing and smoothing surface **356** of porous semiconductor layer **354**. The annealed porous semiconductor layer **354** serves as a template layer for growth of a crystalline epitaxial layer in a subsequent action.

FIG. **3**C illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **244** in the flowchart of FIG. **2** according to one implementation of the present application. In semiconductor structure **344**, crystalline epitaxial layer **358** is formed over porous semiconductor layer **354**. Crystalline epitaxial layer **358** is a thin layer of single-crystal material situated over porous semiconductor layer **354**. In one implementation, crystalline epitaxial layer **358** is formed by chemical vapor deposition (CVD). In various implementations, crystalline epitaxial layer **358** can be formed by any other epitaxy technique known in the art. In the present implementation, crystalline epitaxial layer **358** is a silicon epitaxial layer, and

has thickness T1 from approximately five hundred angstroms (500 Å) to approximately two thousand angstroms (2000 Å). In various implementations, crystalline epitaxial layer **358** may be any other type of crystalline epitaxial layer. In various implementations, more than one crystalline epitaxial layer **358** can be formed. Crystalline epitaxial layer **358** serves as device region for formation of semiconductor devices in subsequent actions.

FIG. **3**D illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with optional action **246** in the flowchart of FIG. **2** according to one implementation of the present application. In semiconductor structure **346** of FIG. **3**D, electrical isolation region **360** is formed at least in crystalline epitaxial layer **358** (shown in FIG. **3**C). In particular, in the example of FIG. **3**D, electrical isolation region **360** extends through crystalline epitaxial layer **358** and into porous semiconductor layer **354**.

Electrical isolation region **360** can be formed by etching through crystalline epitaxial layer **358** and into porous semiconductor layer **354**, then depositing an electrically insulating material. In the present implementation, electrical isolation region **360** is also planarized with the top surface of crystalline epitaxial layer **358**, for example, by using chemical machine polishing (CMP). Electrical isolation region **360** can comprise, for example, silicon dioxide (SiO_2).

In the present implementation, depth D1 of electrical isolation region **360** is greater than thickness T1 of crystalline epitaxial layer **358**. Accordingly, electrical isolation region **360** separates crystalline epitaxial layer **358** of FIG. **3**C into two crystalline epitaxial layers **358***a* and **358***b*. In one implementation, depth D1 of electrical isolation region **360** can be substantially equal to thickness T1. In another implementation, depth D1 of electrical isolation region **360** can be less than thickness T1, such that electrical isolation region **360** extends into crystalline epitaxial layer **358** but not into porous semiconductor layer **354**. In various implementations, locally oxidized silicon (LOCOS) can be used instead of or in addition to electrical isolation region **360**.

Crystalline epitaxial layers **358***a* and **358***b* can also be implanted with a dopant. For example, crystalline epitaxial layers **358***a* and **358***b* can be implanted with boron or other appropriate P-type dopant. In another example, one or both of crystalline epitaxial layers **358***a* and **358***b* can be implanted with phosphorus or other appropriate N-type dopant. One or more masks can be utilized to define portions of crystalline epitaxial layers **358***a* and **358***b* that will be implanted with dopants. In one implementation, crystalline epitaxial layers **358***a* and **358***b* are implanted with a dopant after forming electrical isolation region **360**. In another implementation, crystalline epitaxial layer **358** in FIG. **3**C can be implanted with dopants before forming electrical isolation region **360**. In this implementation, electrical isolation region **360** can be formed in a uniform implant region, between two implant regions having different types or concentrations, and/or where two implant regions overlap.

As described below, electrical isolation region **360** reduces signal interference across crystalline epitaxial layers **358***a* and **358***b*. Electrical isolation region **360** is considered optional in that semiconductor structures according to the present application can be formed without electrical isolation region **360**.

FIG. **3**E illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with actions **248***a* and **248***b* in the flowchart of FIG. **2** according to one implementation of the present application. In semiconductor structure **348** of FIG. **3**E, semiconductor devices **318***a*, **318***b*, and **318***c* are formed in crystalline epitaxial layer **358***a*. Similarly, semiconductor device **304** is formed in crystalline epitaxial layer **358***b*. Electrical isolation region **360** separates semiconductor device **304** from semiconductor devices **318***a*, **318***b*, and **318***c*.

In the present implementation, semiconductor devices **318***a*, **318***b*, and **318***c* are transistors. Semiconductor devices **318***a*, **318***b*, and **318***c* in FIG. **3**E may generally correspond to transistors **118***a*, **118***b*, and **118***c* (or transistors **126***a*, **126***b*, and **126***c*) utilized in RF switch **112** in FIG. **1**. Semiconductor device **318***a* includes source/drain junctions **321***a* and **321***b*, gate **324***a*, lightly doped regions **362***a*, gate oxide **364***a*, and spacers **366***a*. Semiconductor device **318***b* includes source/drain junctions **321***b* and **321***c*, gate **324***b*, lightly doped regions **362***b*, gate oxide **364***b*, and spacers **366***b*. Semiconductor device **318***c* includes source/drain junctions **321***c* and **321***d*, gate **324***c*, lightly doped regions **362***c*, gate oxide **364***c*, and spacers **366***c*. Source/drain junction **321***b* is shared by semiconductor devices **318***a* and **318***b*; source/drain junction **321***c* is shared by semiconductor devices **318***b* and **318***c*.

In the present implementation, semiconductor device **304** is also a transistor. Semiconductor device **304** in FIG. **3**E can be utilized in an amplifier, such as PA **104** (or LNA **108**) in FIG. **1**. Semiconductor device **304** includes source/drain junctions **321***e* and **321***f*, gate **324***d*, lightly doped regions **362***d*, gate oxide **364***d*, and spacers **366***d*.

In one implementation, semiconductor device **304** can be utilized as part of a logic circuit. Semiconductor device **304** is considered optional in that semiconductor structures according to the present application can be formed without semiconductor device **304**.

Gates **324***a*, **324***b*, **324***c*, and **324***d* can comprise, for example, polycrystalline silicon (polySi). Source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* can be implanted with a dopant of a different type than their corresponding crystalline epitaxial layer **358***a* or **358***b*. Lightly doped regions **362***a*, **362***b*, **362***c*, and **362***d* can be implanted with a dopant of the same type as their adjacent source/drain junction, but having a lower concentration. Gate oxides **364***a*, **364***b*, **364***c*, and **364***d* can comprise, for example, silicon dioxide (SiO_2). Spacers **366***a*, **366***b*, **366***c*, and **366***d* can comprise, for example, silicon nitride (SiN).

In the present implementation, depth D2 of source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* is substantially less than thickness T1 of crystalline epitaxial layers **358***a* and **358***b*, such that source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* are not in contact with porous semiconductor layer **354**. In one implementation, source/drain junctions **321***a*, **321***b*, **321***c*, and **321***d* are implanted with an N-type dopant (or a P-type dopant in some implementations) in one action, and source/drain junctions **321***e* and **321***f* are implanted with an N-type dopant (or a P-type dopant in some implementations) in another separate action. In one implementation, source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* are implanted with an N-type dopant (or a P-type dopant in some implementations) concurrently in a single action. In various implementations, silicide can be situated over source/drain junctions **321***a*, **321***b*, **321***c*, and **321***d* and/or gates **324***a*, **324***b*, and **324***c*. In various implementations, semiconductor structure **348** can include more or fewer semiconductor devices in crystalline epitaxial layer **358***a*. In various implementations, crystalline epitaxial layers **358***a* and **358***b* can include diodes, or types of semiconductor devices instead of or in addition to transistors.

Because semiconductor structure **348** includes porous semiconductor layer **354** (for example, a porous silicon layer), semiconductor structure **348** reduces signal leakage (for example, RF signal leakage) from semiconductor devices **318***a*, **318***b*, **318***c*, and **304** to ground. Further, porous semiconductor layer **354** (for example, a porous silicon layer) reduces signal interference (for example, RF signal interference) between the different devices built in crystalline epitaxial layers **358***a* and **358***b*. Pores in porous semiconductor layer **354** decrease its effective dielectric constant and increase its resistivity. In semiconductor structure **348** in FIG. **3**E, porous semiconductor layer **354** has a dielectric constant substantially less than the dielectric constant of substrate **352**. For example, when substrate **352** is a bulk silicon substrate having a dielectric constant of approximately 11.7, porous semiconductor layer **354** has a dielectric constant significantly less than 11.7. In particular, porous semiconductor layer **354** can have a dielectric constant from approximately 2.0 to approximately 4.0. The improved RF isolation that results from the low dielectric constant is especially advantageous for RF switching applications as it reduces signal distortion (i.e. improves linearity). It also results in a more uniform voltage distribution across the OFF state FET stack, increasing its power handling capability.

In semiconductor structure **348** in FIG. **3**E, utilizing porous semiconductor layer **354**, with its low dielectric constant, reduces parasitic capacitance between crystalline epitaxial layer **358***a* and substrate **352**. Accordingly, RF signals are less likely to leak from semiconductor devices **318***a*, **318***b*, and **318***c* in crystalline epitaxial layer **358***a* to substrate **352**. For example, in one implementation, semiconductor devices **318***a*, **318***b*, and **318***c* are transistors utilized to maintain RF switch **112** (shown in FIG. **1**) in an OFF state, and substrate **352** functions as a ground. In their OFF states, transistors **318***a*, **318***b*, and **318***c* create a high resistance path along source/drain junctions **321***a*, **321***b*, **321***c*, and **321***d*, while the RF signals would have been subject to adverse impact of parasitic capacitances with substrate **352** if porous semiconductor layer **354** were not utilized. In other words, the RF signals could easily leak from semiconductor devices **318***a*, **318***b*, and **318***c* to ground, increasing OFF state parasitic capacitance and negatively impacting the performance of semiconductor structure **348**. Where semiconductor devices **318***a*, **318***b*, and **318***c* are transistors utilized to maintain RF switch **112** (shown in FIG. **1**) in an ON state, RF signal leakage, absent porous semiconductor layer **354**, could also result in a higher insertion loss.

Because semiconductor structure **348** includes porous semiconductor layer **354** in combination with electrical isolation region **360**, semiconductor structure **348** also reduces signal interference from semiconductor devices **318***a*, **318***b*, **318***c* to semiconductor device **304**, and vice versa. If porous semiconductor layer **354** and electrical isolation region **360** were not utilized, signals (for example RF signals) from semiconductor device **304** could propagate through crystalline epitaxial layers **358***b* and **358***a* and/or substrate **352**, and interfere with semiconductor devices **318***a*, **318***b*, **318***c* and generate additional undesirable noise in semiconductor devices **318***a*, **318***b*, **318***c*. Where semiconductor device **304** is a transistor utilized in PA **104** (shown in FIG. **1**), these consequences could be amplified. Together, the low dielectric constant of porous semiconductor layer **354** and electrical insulation of electrical isolation region **360** reduce signal leakage and interference through crystalline epitaxial layers **358***a* and **358***b* and/or substrate **352**. The leakage and interference are especially reduced where depth D**1** of electrical isolation region **360** is equal to or greater than thickness T**1** of crystalline epitaxial layers **358***a* and **358***b*.

Semiconductor structure **348** in FIG. **3**E can achieve this reduced signal leakage without using costly materials for substrate **352**, such as quartz or sapphire, and also without requiring costly and/or specialized fabrication techniques used to create trap-rich silicon-on-insulator (SOI) structures, such as smart cut techniques. As described above porous semiconductor layer **354** (for example, a porous silicon layer) can have a dielectric constant from approximately 2.0 to approximately 4.0, comparable to a buried oxide (BOX) in an SOI structure having a dielectric constant of approximately 3.7. Porous semiconductor layer **354** (for example, a porous silicon layer) can be situated over bulk semiconductor substrate **352** (for example, a bulk silicon substrate), and included in semiconductor structure **348** by various fabrication techniques. Thereafter, as discussed above, porous semiconductor layer **354** can be annealed and serve as a high-quality template for growth of crystalline epitaxial layer **358** (shown in FIG. **3**C), in which semiconductor devices **318***a*, **318***b*, **318***c*, and **304** are formed. Further, shallow source/drain junctions **321***a*, **321***b*, **321***c*, and **321***d* improve performance of semiconductor devices **318***a*, **318***b*, and **318***c* by reducing junction capacitances.

FIG. **3**F illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with actions **248***a* and **248***b* in the flowchart of FIG. **2** according to one implementation of the present application. Semiconductor structure **348** of FIG. **3**F represents an alternative implementation to semiconductor structure **348** of FIG. **3**E. Semiconductor structure **348** of FIG. **3**F is similar to semiconductor structure **348** of FIG. **3**E, except that, in semiconductor structure **348** of FIG. **3**F, depth D**3** of source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* is substantially equal to thickness T**1** of crystalline epitaxial layers **358***a* and **358***b*, such that source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* are in contact with porous semiconductor layer **354**. Compared to semiconductor structure **348** of FIG. **3**E, deeper source/drain junctions **321***e* and **321***f* in semiconductor structure **348** of FIG. **3**F improve performance of semiconductor device **304** by improving high current and high voltage handling. Other than the differences described above, semiconductor structure **348** of FIG. **3**F may have any implementations and advantages described above with respect to semiconductor structure **348** of FIG. **3**E.

From the above description it is manifest that various techniques can be used for implementing the concepts described in the present application without departing from the scope of those concepts. Moreover, while the concepts have been described with specific reference to certain implementations, a person of ordinary skill in the art would recognize that changes can be made in form and detail without departing from the scope of those concepts. As such, the described implementations are to be considered in all respects as illustrative and not restrictive. It should also be understood that the present application is not limited to the particular implementations described above, but many rearrangements, modifications, and substitutions are possible without departing from the scope of the present disclosure.

The invention claimed is:

1. A semiconductor structure comprising:

a substrate having a first dielectric constant;

a porous semiconductor layer situated over said substrate;

at least one crystalline epitaxial layer situated directly on said porous semiconductor layer;

a first semiconductor device situated in said at least one crystalline epitaxial layer;

said porous semiconductor layer having a second dielectric constant that is substantially less than said first dielectric constant such that said porous semiconductor layer reduces signal leakage from said first semiconductor device.

2. The semiconductor structure of claim **1**, further comprising:

a second semiconductor device situated in said at least one crystalline epitaxial layer; and

an electrical isolation region separating said first and second semiconductor devices.

3. The semiconductor structure of claim **2**, wherein a depth of said electrical isolation region is equal to or greater than a thickness of said at least one crystalline epitaxial layer.

4. The semiconductor structure of claim **1**, wherein said first semiconductor device is a transistor utilized in a radio frequency (RF) switch.

5. The semiconductor structure of claim **4**, wherein a depth of a source/drain junction of said transistor is substantially less than a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is not in contact with said porous semiconductor layer.

6. The semiconductor structure of claim **4**, wherein a depth of a source/drain junction of said transistor is substantially equal to a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is in contact with said porous semiconductor layer.

7. The semiconductor structure of claim **1**, wherein said substrate comprises a first semiconductor material, and said porous semiconductor layer comprises a semiconductor material selected from one of said first semiconductor material and a second semiconductor material.

8. A semiconductor structure comprising:

a porous silicon layer;

at least one crystalline epitaxial layer situated directly on said porous silicon layer;

first and second transistors situated in said at least one crystalline epitaxial layer;

an electrical isolation region separating said first and second transistors.

9. The semiconductor structure of claim **8**, wherein said porous silicon layer is situated over a bulk silicon substrate.

10. The semiconductor structure of claim **8**, wherein a depth of said electrical isolation region is equal to or greater than a thickness of said at least one crystalline epitaxial layer.

11. The semiconductor structure of claim **8**, wherein said first transistor is utilized in a radio frequency (RF) switch.

12. The semiconductor structure of claim **8**, wherein a depth of a source/drain junction of said first transistor is substantially less than a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is not in contact with said porous silicon layer.

13. The semiconductor structure of claim **8**, wherein a depth of a source/drain junction of said first transistor is substantially equal to a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is in contact with said porous silicon layer.

14. A semiconductor structure comprising:

a porous semiconductor layer situated over a substrate, said porous semiconductor layer having a higher resistivity than said substrate;

at least one crystalline epitaxial layer situated directly on said porous semiconductor layer;

a first semiconductor device situated in said at least one crystalline epitaxial layer.

15. The semiconductor structure of claim **14**, wherein said substrate comprises a first semiconductor material, and said porous semiconductor layer comprises said first semiconductor material.

16. The semiconductor structure of claim **14**, wherein said substrate comprises a first semiconductor material, and said porous semiconductor layer comprises a second semiconductor material.

17. The semiconductor structure of claim **14**, further comprising:

a second semiconductor device situated in said at least one crystalline epitaxial layer; and

an electrical isolation region separating said first and second semiconductor devices.

18. The semiconductor structure of claim **17**, wherein a depth of said electrical isolation region is equal to or greater than a thickness of said at least one crystalline epitaxial layer.

19. The semiconductor structure of claim **14**, wherein said first semiconductor device is a transistor utilized in a radio frequency (RF) switch.

20. The semiconductor structure of claim **19**, wherein a depth of a source/drain junction of said transistor is substantially less than a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is not in contact with said porous semiconductor layer.

* * * * *

Exhibit 3

US011195920B2

(12) **United States Patent**
Hurwitz et al.

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(45) **Date of Patent: Dec. 7, 2021**

(54) **SEMICONDUCTOR STRUCTURE HAVING POROUS SEMICONDUCTOR SEGMENT FOR RF DEVICES AND BULK SEMICONDUCTOR REGION FOR NON-RF DEVICES**

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(72) Inventors: **Paul D. Hurwitz**, Irvine, CA (US); **Edward Preisler**, San Clemente, CA (US); **David J. Howard**, Irvine, CA (US); **Marco Racanelli**, Santa Ana, CA (US)

(73) Assignee: **Newport Fab, LLC**, Newport Beach, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(65) **Prior Publication Data**

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Related U.S. Application Data

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H01L 23/66 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H01L 29/1083*** (2013.01); ***H01L 21/02428*** (2013.01); ***H01L 21/324*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC ... H01L 29/1083; H01L 23/66; H01L 21/324; H01L 21/02428; H01L 27/088; H01L 29/10; H01L 21/02; H01L 21/02532; H01L 21/02667; H01L 21/76224; H01L 2223/6688
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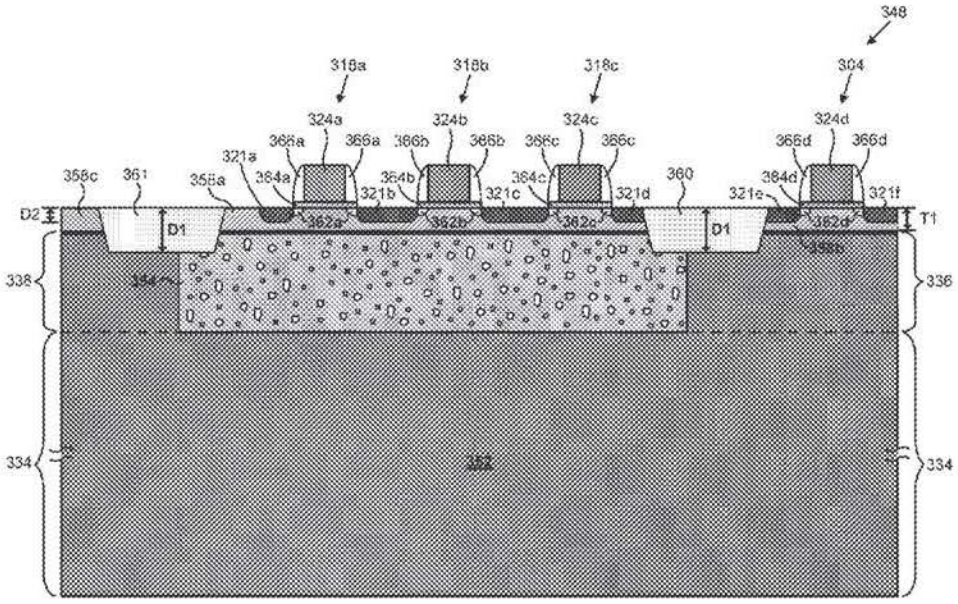
Primary Examiner — Alexander O Williams
(74) *Attorney, Agent, or Firm* — Farjami & Farjami LLP

(57) **ABSTRACT**

A semiconductor structure includes a porous semiconductor segment adjacent to a first region of a substrate, and a crystalline epitaxial layer situated over the porous semiconductor segment and over the first region of the substrate. A first semiconductor device is situated in the crystalline epitaxial layer over the porous semiconductor segment. The first region of the substrate has a first dielectric constant, and the porous semiconductor segment has a second dielectric constant that is substantially less than the first dielectric constant such that the porous semiconductor segment reduces signal leakage from the first semiconductor device. The semiconductor structure can include a second semiconductor device situated in the crystalline epitaxial layer over the first region of the substrate, and an electrical isolation region separating the first and second semiconductor devices.

19 Claims, 8 Drawing Sheets



(51) **Int. Cl.**
H01L 21/324 (2006.01)
H01L 27/088 (2006.01)
H01L 21/02 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 23/66*** (2013.01); ***H01L 27/088*** (2013.01); *H01L 2223/6688* (2013.01)

(58) **Field of Classification Search**
USPC 257/347
See application file for complete search history.

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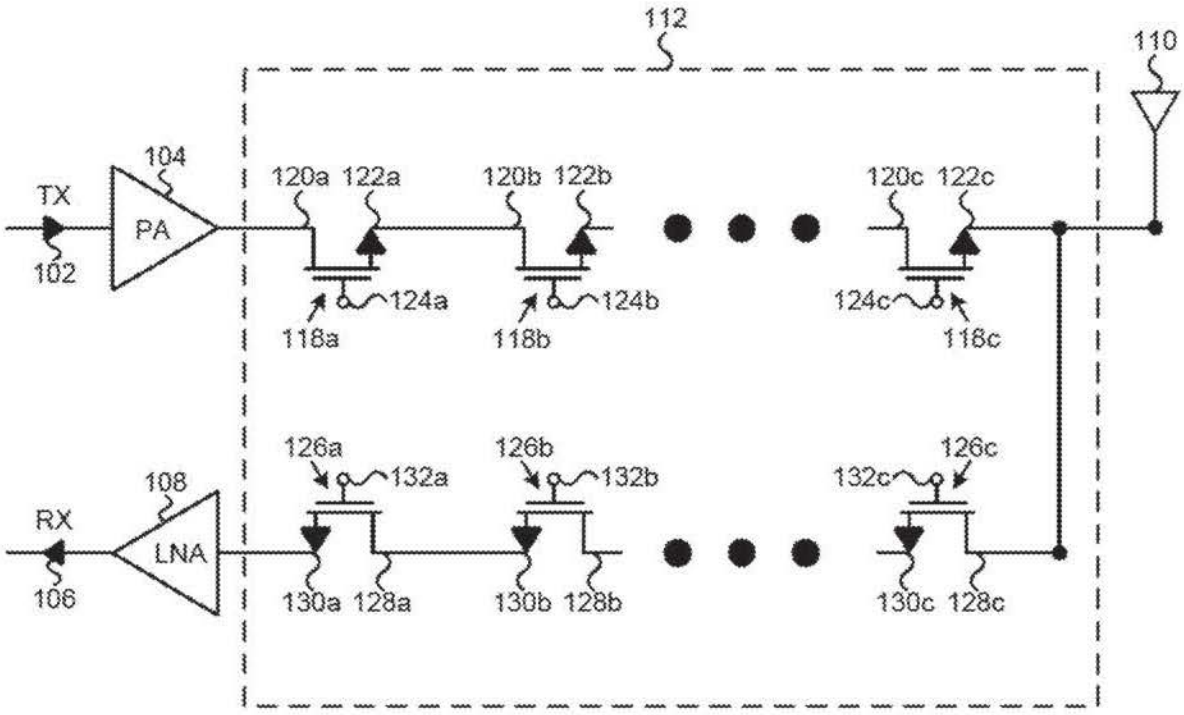
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120a 122a
120b 122b
120c 122c
124a
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118b
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132c
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LNA
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130c 128c

FIG. 1

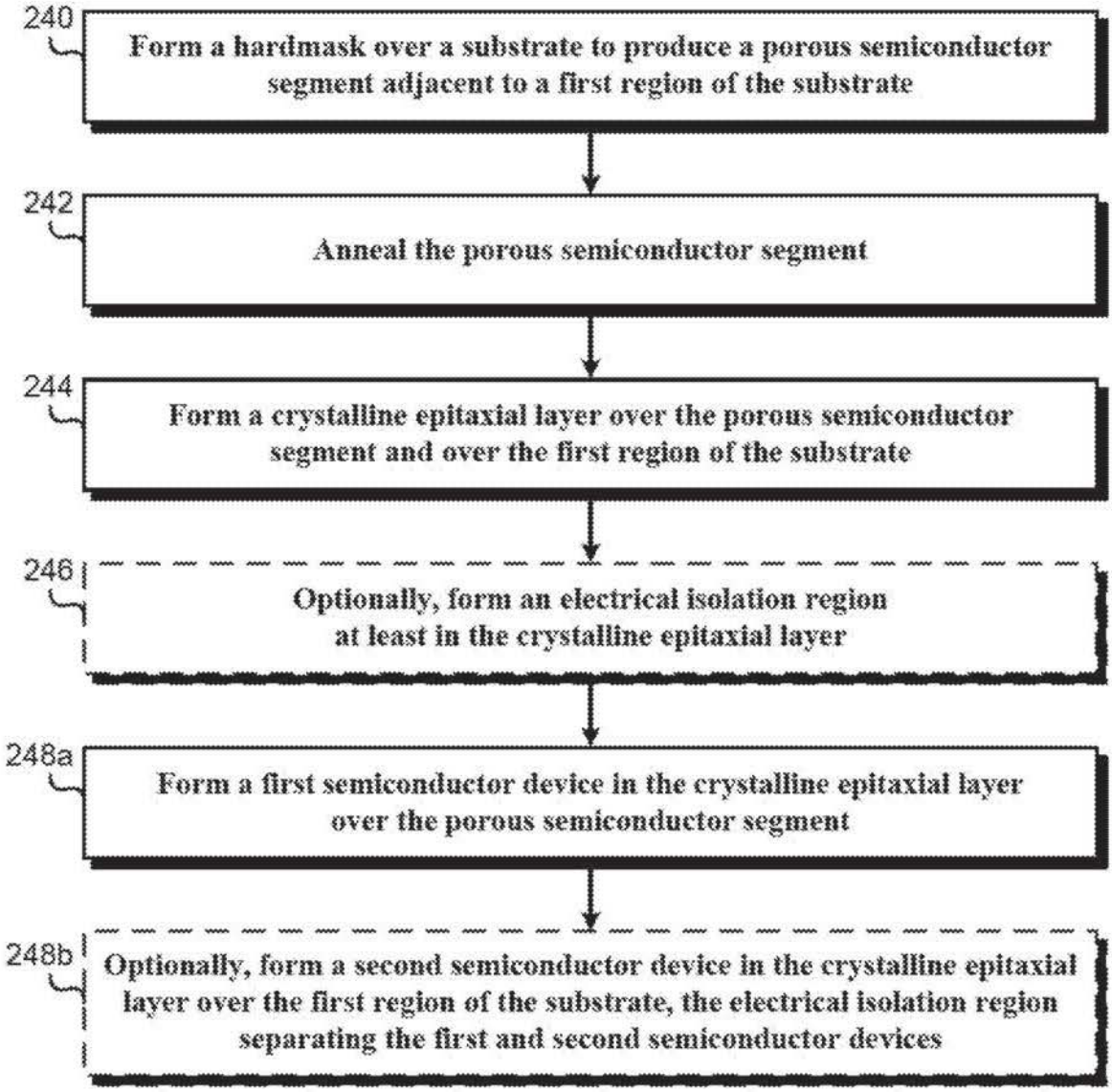
240
Form a hardmask over a substrate to produce a porous semiconductor segment adjacent to a first region of the substrate
242
Anneal the porous semiconductor segment
244
Form a crystalline epitaxial layer over the porous semiconductor segment and over the first region of the substrate
246
Optionally, form an electrical isolation region at least in the crystalline epitaxial layer
248a
Form a first semiconductor device in the crystalline epitaxial layer over the porous semiconductor segment
248b
Optionally, form a second semiconductor device in the crystalline epitaxial layer over the first region of the substrate, the electrical isolation region separating the first and second semiconductor devices

FIG. 2

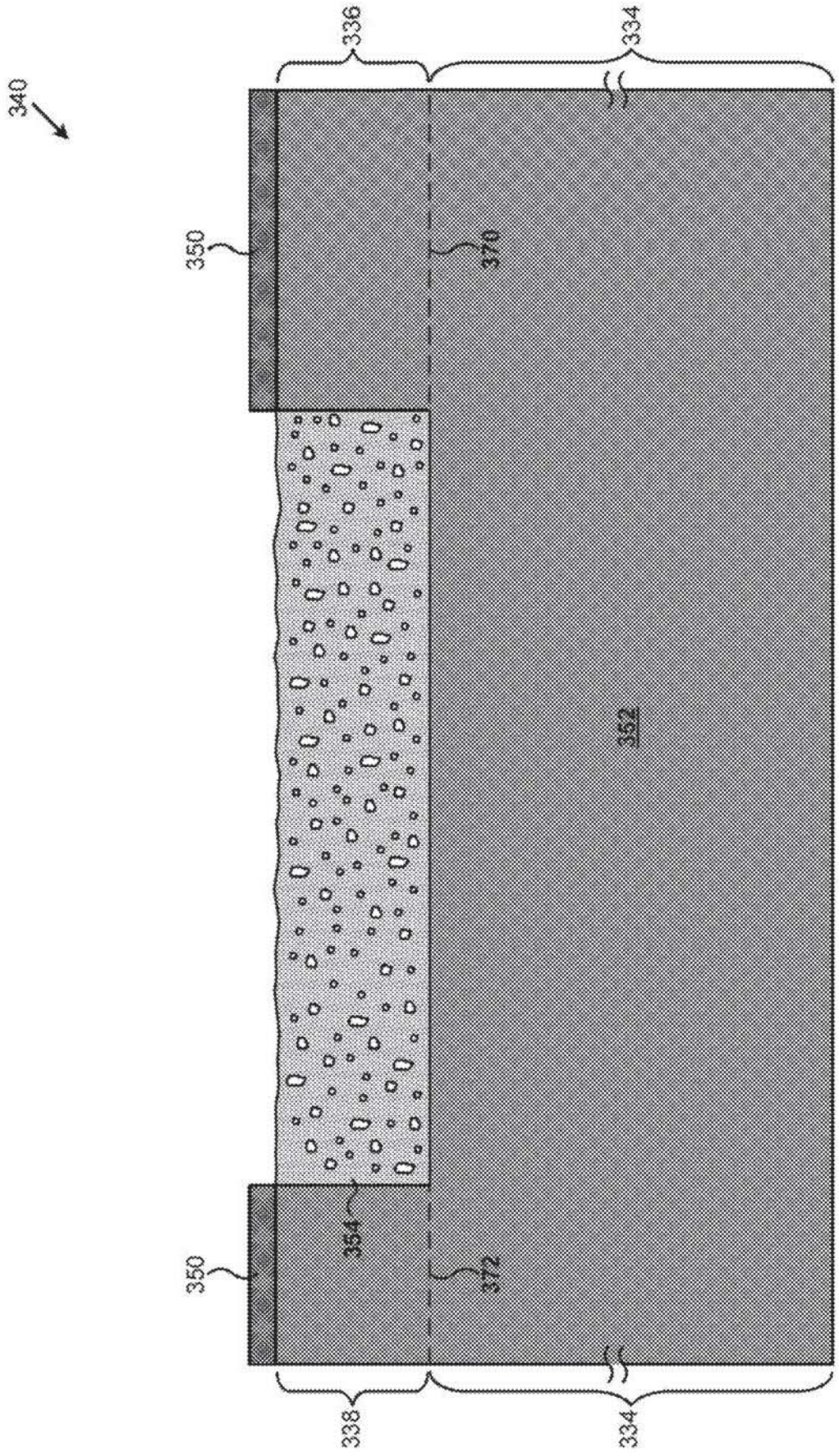

FIG. 3A

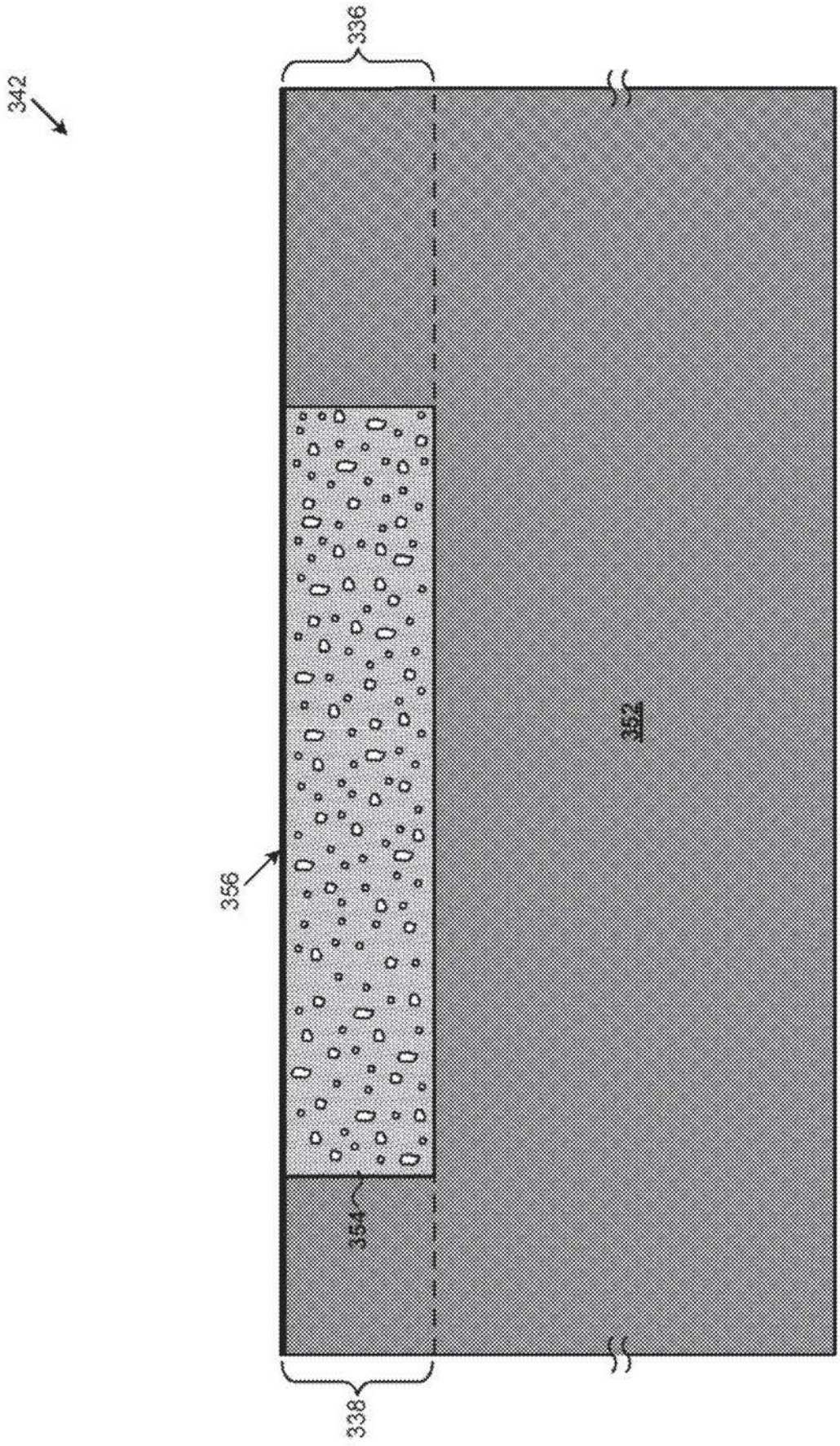

FIG. 3B

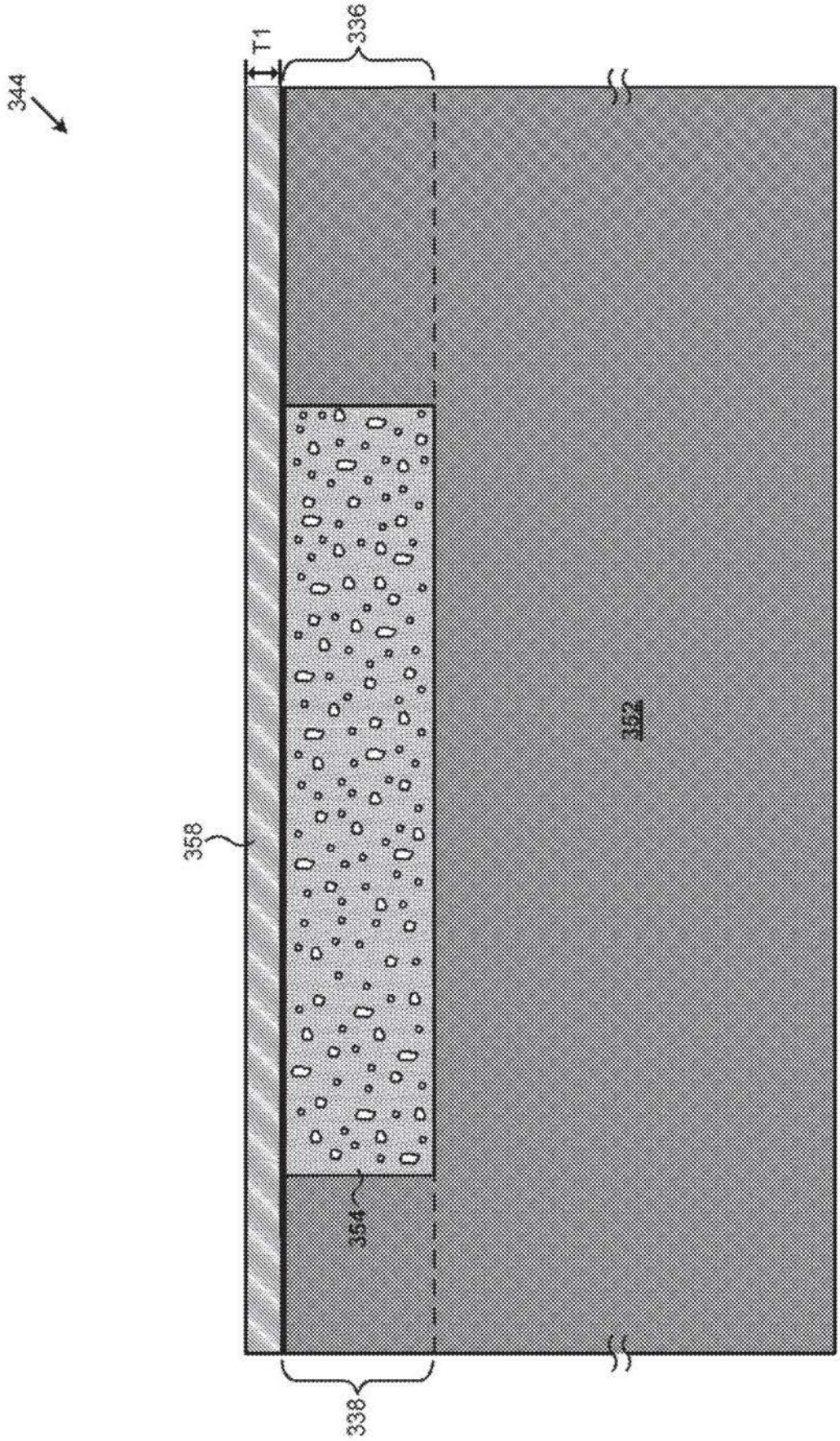

FIG. 3C

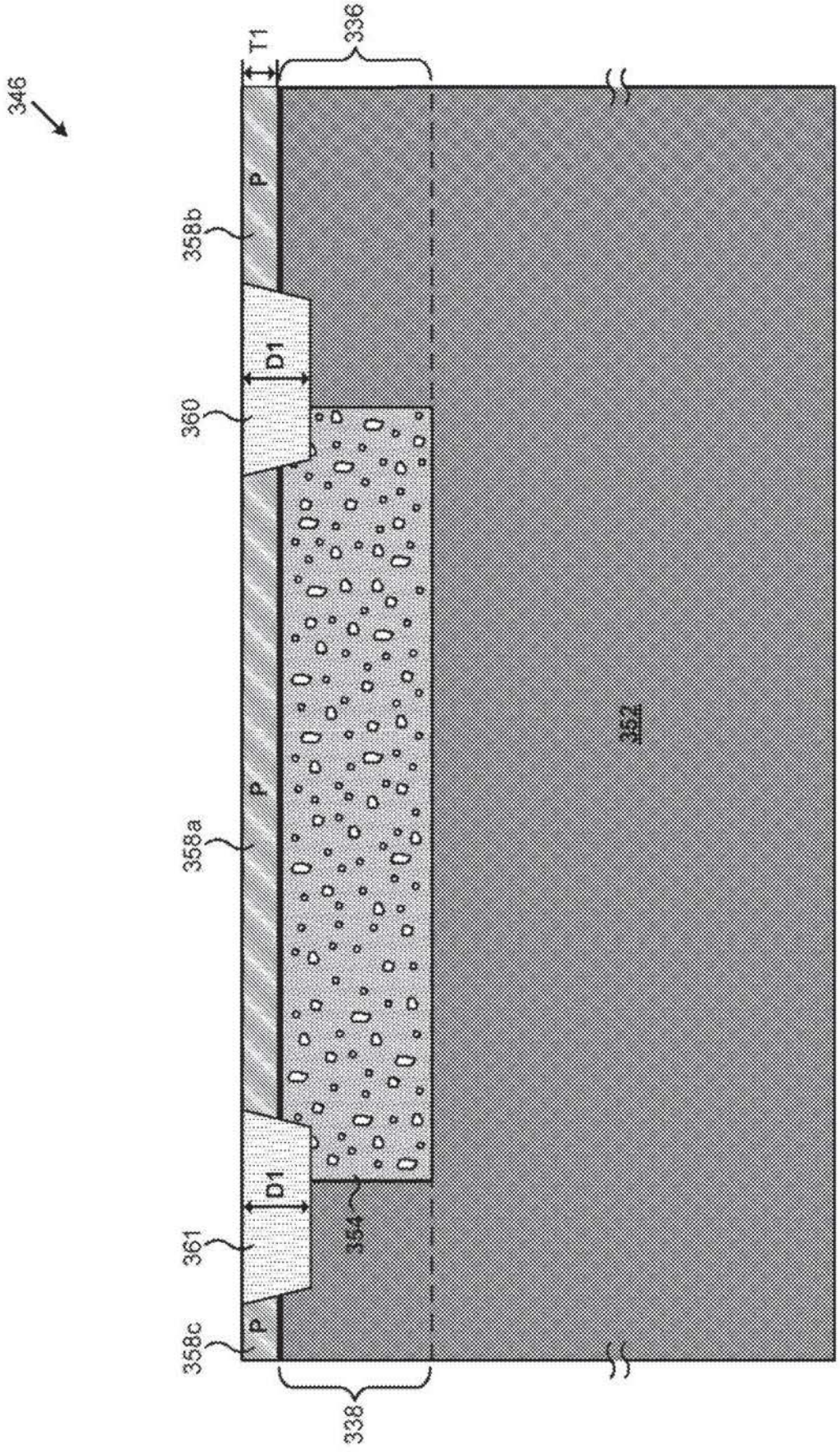

FIG. 3D

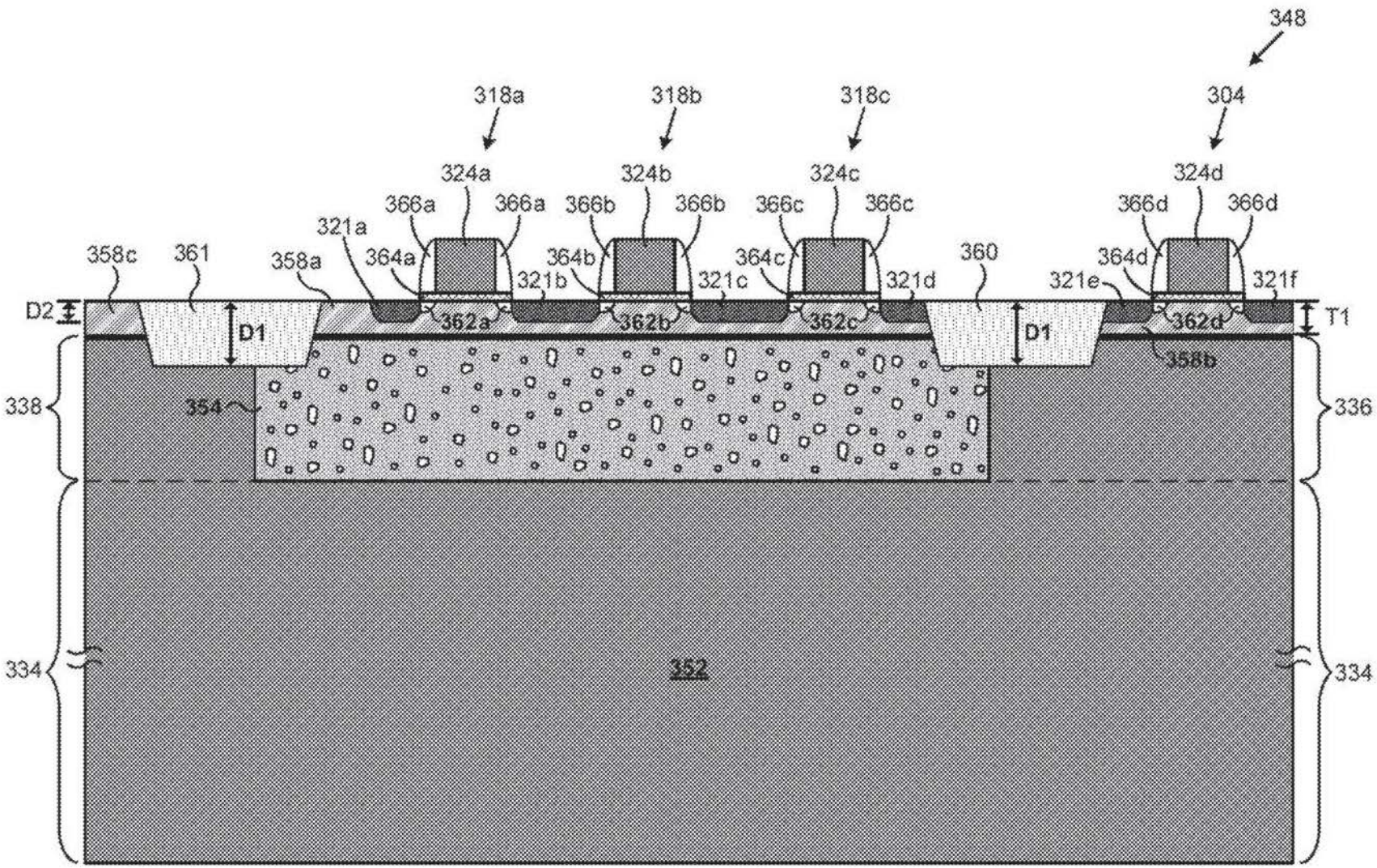
348
318a
318b
318c
304
324a
324b
324c
324d
366a
366b
366c
366d
321a
358c
361
358a
364a
364b
364c
364d
360
321b
321c
321d
321e
321f
D2
D1
362a
362b
362c
362d
T1
358b
338
354
336
334
352

FIG. 3E

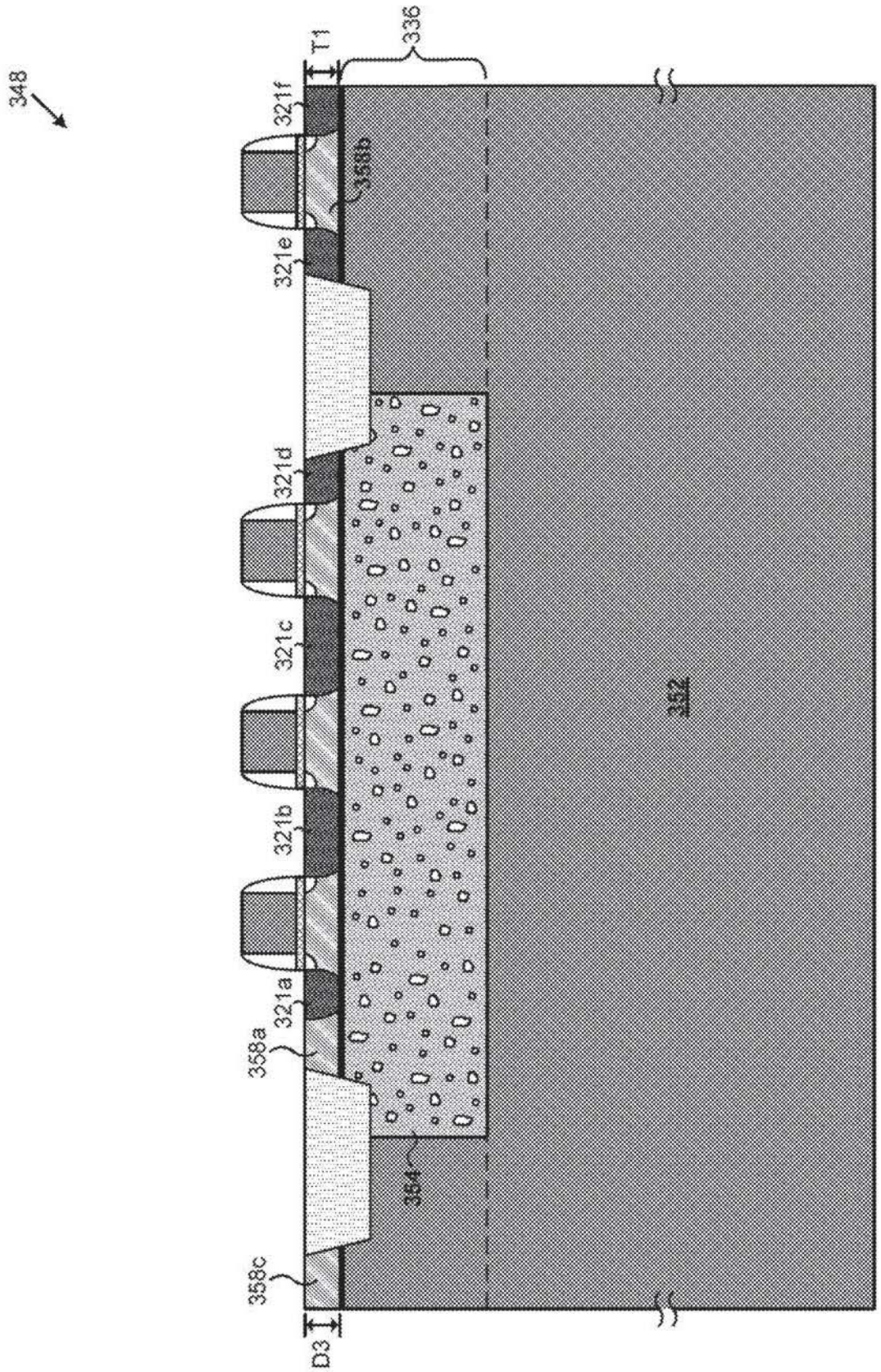
348
T1
336
321f
358b
321e
321d
321c
321b
321a
358a
354
358c
D3
352

FIG. 3F

SEMICONDUCTOR STRUCTURE HAVING POROUS SEMICONDUCTOR SEGMENT FOR RF DEVICES AND BULK SEMICONDUCTOR REGION FOR NON-RF DEVICES

CLAIMS OF PRIORITY

The present application is a continuation-in-part of and claims the benefit of and priority to application Ser. No. 16/597,779 filed on Oct. 9, 2019 and titled "Semiconductor Structure Having Porous Semiconductor Layer for RF Devices,". The disclosure and content of the above-identified application are hereby incorporated fully by reference into the present application.

BACKGROUND

Semiconductor-on-insulator (SOI) structures are commonly employed to realize radio frequency (RF) designs where low signal leakage is required. These SOI structures use a buried oxide (BOX) under a top device layer in which RF circuit components, such as transistors and/or passive components, are fabricated.

As known in the art, a handle wafer functioning as a substrate under the BOX results in some signal leakage. In one approach, a high resistivity silicon is used for the handle wafer in order to improve isolation and reduce signal loss. However, the relatively high dielectric constant of silicon (k=11.7) results in significant capacitive loading of RF SOI devices. In another approach, a trap-rich layer is formed between the handle wafer and the BOX in order to minimize parasitic surface conduction effects that would adversely affect RF devices in the top device layer. However, this approach requires costly and/or specialized fabrication techniques.

Further, due to existence of the BOX in SOI structures, each CMOS device built in the top device layer is dielectrically isolated from the substrate. To control the body potential (avoid floating body effects, and hysteresis) each device requires its own body contact. This approach results in the consumption of much of the surface area in a die, decreasing logic density in the die. Further, the BOX has much low thermal conductivity compared to monocrystalline silicon (approximately one and half watts per meter-kelvin (1.5 W/(m·K)) versus approximately one hundred and fifty watts per meter-kelvin (150 W/(m·K)) respectively). As a result, high power components, such as power amplifiers, integrated in SOI structures cannot effectively dissipate heat.

Thus, there is need in the art for efficiently and effectively fabricating semiconductor dies with reduced RF signal leakage, reduced need for numerous body contacts, and increased heat dissipation at low cost.

SUMMARY

The present disclosure is directed to a semiconductor structure having at least one porous semiconductor segment for radio frequency (RF) devices and at least one bulk semiconductor region for non-RF devices, substantially as shown in and/or described in connection with at least one of the figures, and as set forth in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates a portion of a transceiver including a radio frequency (RF) switch employing stacked transistors according to one implementation of the present application.

FIG. **2** illustrates a portion of a flowchart of an exemplary method for manufacturing a semiconductor structure according to one implementation of the present application.

FIG. **3**A illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **240** in the flowchart of FIG. **2** according to one implementation of the present application.

FIG. **3**B illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **242** in the flowchart of FIG. **2** according to one implementation of the present application

FIG. **3**C illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **244** in the flowchart of FIG. **2** according to one implementation of the present application

FIG. **3**D illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **246** in the flowchart of FIG. **2** according to one implementation of the present application.

FIG. **3**E illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with actions **248***a* and **248***b* in the flowchart of FIG. **2** according to one implementation of the present application.

FIG. **3**F illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with actions **248***a* and **248***b* in the flowchart of FIG. **2** according to one implementation of the present application.

DETAILED DESCRIPTION

The following description contains specific information pertaining to implementations in the present disclosure. The drawings in the present application and their accompanying detailed description are directed to merely exemplary implementations. Unless noted otherwise, like or corresponding elements among the figures may be indicated by like or corresponding reference numerals. Moreover, the drawings and illustrations in the present application are generally not to scale, and are not intended to correspond to actual relative dimensions.

FIG. **1** illustrates a portion of a radio front-end of a transceiver (hereinafter referred to simply as a "transceiver") including a radio frequency (RF) switch employing stacked transistors according to one implementation of the present application. The transceiver in FIG. **1** includes transmit input **102**, power amplifier (PA) **104**, receive output **106**, low-noise amplifier (LNA) **108**, antenna **110**, and radio frequency (RF) switch **112**.

RF switch **112** is situated between PA **104** and antenna **110**. PA **104** amplifies RF signals transmitted from transmit input **102**. In one implementation, transmit input **102** can be coupled to a mixer (not shown in FIG. **1**), or to another input source. The output of PA **104** is coupled to one end of RF switch **112**. A matching network (not shown in FIG. **1**) can be coupled between PA **104** and RF switch **112**. Another end of RF switch **112** is coupled to antenna **110**. Antenna **110** can transmit amplified RF signals. In one implementation, RF switch **112** can be coupled to an antenna array, rather than a single antenna **110**.

RF switch **112** is also situated between LNA **108** and antenna **110**. Antenna **110** also receives RF signals. Antenna **110** is coupled to one end of RF switch **112**. Another end of RF switch **112** is coupled to the input of LNA **108**. LNA **108** amplifies RF signals received from RF switch **112**. A matching network (not shown in FIG. **1**) can be coupled between RF switch **112** and LNA **108**. Receive output **106** receives amplified RF signals from LNA **108**. In one implementation,

receive output **106** can be coupled to a mixer (not shown in FIG. **1**), or to another output source.

RF switch **112** includes two stacks of transistors. The first stack includes transistors **118***a*, **118***b*, and **118***c*. Drain **120***a* of transistor **118***a* is coupled to the output of PA **104**. Source **122***a* of transistor **118***a* is coupled to drain **120***b* of transistor **118***b*. Source **122***b* of transistor **118***b* can be coupled to the drain of additional transistors, and ultimately coupled to drain **120***c* of transistor **118***c*. Source **122***c* of transistor **118***c* is coupled to antenna **110**. Gates **124***a*, **124***b*, and **124***c* of transistors **118***a*, **118***b*, and **118***c* respectively can be coupled to a controller or a pulse generator (not shown) for switching transistors **118***a*, **118***b*, and **118***c* between ON and OFF states.

The second stack includes transistors **126***a*, **126***b*, and **126***c*. Source **130***a* of transistor **126***a* is coupled to the input of LNA **108**. Drain **128***a* of transistor **126***a* is coupled to source **130***b* of transistor **126***b*. Drain **128***b* of transistor **126***b* can be coupled to the drain of additional transistors, and ultimately coupled to drain source **130***c* of transistor **126***c*. Drain **128***c* of transistor **126***c* is coupled to antenna **110**. Gates **132***a*, **132***b*, and **132***c* of transistors **126***a*, **126***b*, and **126***c* respectively can be coupled to a controller or a pulse generator (not shown) for switching transistors **126***a*, **126***b*, and **126***c* between ON and OFF states.

In the example of FIG. **1**, RF switch **112** switches the transceiver in FIG. **1** between receive and transmit modes. When transistors **118***a*, **118***b*, and **118***c* are in OFF states, and transistors **126***a*, **126***b*, and **126***c* are in ON states, the transceiver is in receive mode. Transistors **126***a*, **126***b*, and **126***c* serve as a receive path for RF signals received by antenna **110** to pass to LNA **108** and to receive output **106**. When transistors **118***a*, **118***b*, and **118***c* are in ON states, and transistors **126***a*, **126***b*, and **126***c* are in OFF states, the transceiver is in transmit mode. Transistors **118***a*, **118***b*, and **118***c* serve as a transmit path for RF signals transmitted from transmit input **102** and PA **104** to pass to antenna **110**. In various implementations, RF switch **112** can include more stacks of transistors and/or more amplifiers. In various implementations, RF switch **112** can switch the transceiver between two transmit modes corresponding to different frequencies, or between two receive modes corresponding to different frequencies.

In the present implementation, transistors **118***a*, **118***b*, **118***c*, **126***a*, **126***b*, and **126***c* are N-type field effect transistors (NFETs). In various implementations, transistors **118***a*, **118***b*, **118***c*, **126***a*, **126***b*, and **126***c* can be P-type FETs (PFETs), junction FETs (JFETs), or any other type of transistor. By stacking transistors **118***a*, **118***b*, **118***c*, **126***a*, **126***b*, and **126***c* as shown in FIG. **1**, the overall OFF state power and voltage handling capability for RF switch **112** can be increased. For example, if only transistors **118***a* and **126***a* were used, RF switch **112** may have an OFF-state voltage handling capability of five volts (5 V). If eight transistors were used in each stack, RF switch **112** may have an OFF-state voltage handling capability of forty volts (40 V). In various implementations. RF switch **112** can have more or fewer stacked transistors than shown in FIG. **1**.

As described above, in conventional semiconductor structures, RF signals can leak from RF switch **112**, for example, to ground or to other devices. This RF signal leakage is particularly problematic when transistors **118***a*, **118***b*, **118***c*, **126***a*, **126***b*, and **126***c* are in OFF states, and when dealing with higher frequency RF signals. According to the present application, RF switch **112** can be utilized in a semiconductor structure that reduces RF signal leakage. It is noted that, although the present application focuses on RF signals, the signals may have frequencies other than RF frequencies.

As also described above, conventional semiconductor structures cannot easily accommodate body contacts without tradeoffs, and cannot effectively dissipate heat from high power devices, such as PA **104**, integrated with RF switch **112**. According to the present application. RF switch **112** can be utilized in a semiconductor structure that integrates PA **104** (and/or LNA **108**) while easily accommodating body contacts and providing effective heat dissipation therefor.

FIG. **2** illustrates a portion of a flowchart of an exemplary method for manufacturing a semiconductor structure according to one implementation of the present application. Structures shown in FIGS. **3**A through **3**E illustrate the results of performing actions **240** through **248***b* shown in the flowchart of FIG. **2**. For example, FIG. **3**A shows a semiconductor structure after performing action **240** in FIG. **2**, FIG. **3**B shows a semiconductor structure after performing action **242** in FIG. **2**, and so forth.

Actions **240** through **248***b* shown in the flowchart of FIG. **2** are sufficient to describe one implementation of the present inventive concepts. Other implementations of the present inventive concepts may utilize actions different from those shown in the flowchart of FIG. **2**. Certain details and features have been left out of the flowchart of FIG. **2** that are apparent to a person of ordinary skill in the art. For example, an action may consist of one or more sub-actions or may involve specialized equipment or materials, as known in the art. Moreover, some actions, such as masking and cleaning actions, are omitted so as not to distract from the illustrated actions.

FIG. **3**A illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **240** in the flowchart of FIG. **2** according to one implementation of the present application. As shown in FIG. **3**A, according to action **240**, semiconductor structure **340** includes hardmask **350** formed over bulk silicon substrate **352** to produce porous silicon segment **354** adjacent to regions **336** and **338** of bulk silicon substrate **352**.

Bulk silicon substrate **352** includes regions **334**, **336**, and **338**. Region **334** is situated under porous silicon segment **354** and under regions **336** and **338**. Regions **336** and **338** are adjacent to porous silicon segment **354** on respective sides. In FIG. **3**A, dashed line **370** illustrates the boundary of regions **334** and **336**, and dashed line **372** illustrates the boundary of regions **334** and **338**. It is understood that dashed lines **370** and **372** merely illustrate conceptual boundaries of regions **334**, **336**, and **338**, and that regions **334**, **336**, and **338** of bulk silicon substrate **352** is typically one continuous bulk semiconductor material. In the present implementation, bulk silicon substrate **352** is a P– or P+ type bulk silicon substrate having a thickness of approximately seven hundred microns (700 μm). In various implementations, bulk silicon substrate **352** may be any other type of substrate.

Porous silicon segment **354** adjacent to regions **336** and **338** and situated over region **334** is a silicon segment having voids, or pores, therein. Within porous silicon segment **354**, the pores can have any orientation, branching, fill, or other morphological characteristic known in the art. Porous silicon segment **354** can be formed by using a top-down technique, where portions of bulk silicon substrate **352** are removed to generate pores. In the present implementation, hardmask **350** is formed over bulk silicon substrate **352** to expose a segment thereof. Then, porous silicon segment **354** is formed by electrochemical etching the exposed segment of bulk silicon substrate **352** using hydrofluoric acid (HF).

Hardmask **350** can comprise, for example, silicon nitride (SiN). Alternatively, porous silicon segment **354** can also be formed by stain etching, photoetching, or any other top-down technique known in the art.

Porous silicon segment **354** can also be formed by using a bottom-up technique, where deposition results in a silicon segment having voids. For example, a trench can be etched in bulk silicon substrate **352**. Then, a porous silicon layer can be formed by low-temperature high-density plasma (HDP) deposition. Then, porous silicon segment **354** can be formed by removing portions of the porous silicon layer outside the trench, for example, using chemical machine polishing (CMP). Alternatively, the porous silicon layer can also be formed by plasma hydrogenation of an amorphous layer, laser ablation, or any other bottom-up technique known in the art. In the present implementation, porous silicon segment **354** has a thickness from approximately ten microns (10 μm) to approximately fifty microns (50 μm). In various implementations, porous silicon segment **354** can have any other thickness. In various implementations, porous segment **354** may be a semiconductor material other than silicon.

FIG. **3**B illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **242** in the flowchart of FIG. **2** according to one implementation of the present application. In semiconductor structure **342**, porous silicon segment **354** is annealed. For example, porous silicon segment **354** can be annealed in argon (Ar) or hydrogen (H_2) at atmospheric pressure from a temperature of approximately seven hundred degrees Celsius (700° C.) to a temperature of approximately eleven hundred degrees Celsius (1100° C.) for approximately ten minutes (10 min). Any other annealing technique known in the art can be utilized, such as techniques utilizing different temperatures, durations, and/or pressures. The annealing shown in FIG. **3**B reorganizes the pores in porous silicon segment **354** into larger cavities, while closing and smoothing surface **356**. The annealed porous silicon segment **354**, along with regions **336** and **338** of bulk silicon substrate **352**, serves as a template layer for growth of a crystalline epitaxial layer in a subsequent action.

FIG. **3**C illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **244** in the flowchart of FIG. **2** according to one implementation of the present application. In semiconductor structure **344**, crystalline epitaxial layer **358** is formed over porous silicon segment **354** and over regions **336** and **338** of bulk silicon substrate **352**. Crystalline epitaxial layer **358** is a thin layer of single-crystal material. In one implementation, crystalline epitaxial layer **358** is formed by chemical vapor deposition (CVD). In various implementations, crystalline epitaxial layer **358** can be formed by any other epitaxy technique known in the art. In the present implementation, crystalline epitaxial layer **358** is a silicon epitaxial layer, and has thickness T**1** from approximately five hundred angstroms (500 Å) to approximately two thousand angstroms (2000 Å). In various implementations, crystalline epitaxial layer **358** may be any other type of crystalline epitaxial layer. In various implementations, more than one crystalline epitaxial layer **358** can be formed. Crystalline epitaxial layer **358** serves as device region for formation of semiconductor devices in subsequent actions.

FIG. **3**D illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with optional action **246** in the flowchart of FIG. **2** according to one implementation of the present application. In semiconductor structure **346** of FIG. **3**D, electrical isolation regions **360** and **361** are formed at least in crystalline epitaxial layer **358** (shown in FIG. **3**C). In particular, in the example of FIG. **3**D, electrical isolation region **360** extends through crystalline epitaxial layer **358**, into porous silicon segment **354** and region **336** of bulk silicon substrate **352**. Similarly, electrical isolation region **361** extends through crystalline epitaxial layer **358**, into porous silicon segment **354** and region **338** of bulk silicon substrate **352**.

Electrical isolation region **360** can be formed by etching through crystalline epitaxial layer **358**, into porous silicon segment **354** and region **336** of bulk silicon substrate **352**, then depositing an electrically insulating material. Similarly, electrical isolation region **361** can be formed by etching through crystalline epitaxial layer **358**, into porous silicon segment **354** and region **338** of bulk silicon substrate **352**, then depositing an electrically insulating material. In the present implementation, electrical isolation regions **360** and **361** are also planarized with the top surface of crystalline epitaxial layer **358**, for example, by using CMP. Electrical isolation regions **360** and **361** can comprise, for example, silicon dioxide (SiO_2). In the present implementation, depth D**1** of electrical isolation regions **360** and **361** is greater than thickness T**1** of crystalline epitaxial layer **358**. Accordingly, electrical isolation regions **360** and **361** separate crystalline epitaxial layer **358** of FIG. **3**C into three crystalline epitaxial layers **358***a*, **358***b*, and **358***c*.

In one implementation, depth D**1** of electrical isolation regions **360** and **361** can be substantially equal to thickness T**1**. In another implementation, depth D**1** of electrical isolation regions **360** and **361** can be less than thickness T**1**, such that electrical isolation regions **360** and **361** extend into crystalline epitaxial layer **358**, but not into porous silicon segment **354** or regions **336** and **338** of bulk silicon substrate **352**. In various implementations, locally oxidized silicon (LOCOS) can be used instead of or in addition to electrical isolation regions **360** and **361**. In various implementations, electrical isolation regions **360** and **361** can extend into porous silicon segment **354**, but not into regions **336** and **338** of bulk silicon substrate **352**, or vice versa. In various implementations, semiconductor structure **346** includes additional electrical isolation regions.

Crystalline epitaxial layers **358***a*, **358***b*, and **358***c* can also be implanted with a dopant. In the present implementation, crystalline epitaxial layers **358***a*, **358***b*, and **358***c* are implanted with boron or other appropriate P-type dopant. In another implementation, one, two, or all of crystalline epitaxial layers **358***a*, **358***b*, and **358***c* can be implanted with phosphorus or other appropriate N-type dopant. One or more masks can be utilized to define portions of crystalline epitaxial layers **358***a*, **358***b*, and **358***c* that will be implanted with dopants. In one implementation, crystalline epitaxial layers **358***a*, **358***b*, and **358***c* are implanted with a dopant after forming electrical isolation regions **360** and **361**. In another implementation, crystalline epitaxial layer **358** in FIG. **3**C can be implanted with dopants before forming electrical isolation regions **360** and **361**. In this implementation, electrical isolation regions **360** and **361** can be formed in a uniform implant region, between two implant regions having different types or concentrations, and/or where two implant regions overlap.

As described below, electrical isolation regions **360** and **361** reduce RF signal interference across crystalline epitaxial layers **358***a*, **358***b*, and **358***c*. Electrical isolation regions **360** and **361** are considered optional in that semiconductor structures according to the present application can be formed without electrical isolation regions **360** and **361**.

FIG. 3E illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with actions **248***a* and **248***b* in the flowchart of FIG. **2** according to one implementation of the present application. In semiconductor structure **348** of FIG. 3E, transistors **318***a*, **318***b*, and **318***c* are formed in crystalline epitaxial layer **358***a*. Similarly, transistor **304** is formed in crystalline epitaxial layer **358***b*. Electrical isolation region **360** separates transistor **304** from transistors **318***a*, **318***b*, and **318***c*.

Transistors **318***a*, **318***b*, and **318***c* in FIG. 3E may generally correspond to transistors **118***a*, **118***b*, and **118***c* (or transistors **126***a*, **126***b*, and **126***c*) utilized in RF switch **112** in FIG. **1**. Transistor **318***a* includes source/drain junctions **321***a* and **321***b*, gate **324***a*, lightly doped regions **362***a*, gate oxide **364***a*, and spacers **366***a*. Transistor **318***b* includes source/drain junctions **321***b* and **321***c*, gate **324***b*, lightly doped regions **362***b*, gate oxide **364***b*, and spacers **366***b*. Transistor **318***c* includes source/drain junctions **321***c* and **321***d*, gate **324***c*, lightly doped regions **362***c*, gate oxide **364***c*, and spacers **366***c*. Source/drain junction **321***b* is shared by semiconductor devices **318***a* and **318***b*; source/drain junction **321***c* is shared by semiconductor devices **318***b* and **318***c*.

Transistor **304** in FIG. 3E can be utilized in an amplifier, such as PA **104** (or LNA **108**) in FIG. **1**. Transistor **304** includes source/drain junctions **321***e* and **321***f*, gate **324***d*, lightly doped regions **362***d*, gate oxide **364***d*, and spacers **366***d*. In one implementation, transistor **304** can be utilized as part of a logic circuit. Transistor **304** is considered optional in that semiconductor structures according to the present application can be formed without transistor **304**.

Gates **324***a*, **324***b*, **324***c*, and **324***d* can comprise, for example, polycrystalline silicon (polySi). Source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* can be implanted with a dopant of a different type than their corresponding crystalline epitaxial layer **358***a* or **358***b*. Lightly doped regions **362***a*, **362***b*, **362***c*, and **362***d* can be implanted with a dopant of the same type as their adjacent source/drain junction, but having a lower concentration. Gate oxides **364***a*, **364***b*, **364***c*, and **364***d* can comprise, for example, silicon dioxide (SiO_2). Spacers **366***a*, **366***b*, **366***c*, and **366***d* can comprise, for example, silicon nitride (SiN).

In the present implementation, depth D2 of source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* is substantially less than thickness T1 of crystalline epitaxial layers **358***a*, **358***b*, and **358***c*, such that source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* are not in contact with porous silicon segment **354**. In one implementation, source/drain junctions **321***a*, **321***b*, **321***c*, and **321***d* are implanted with an N-type dopant (or a P-type dopant in some implementations) in one action, and source/drain junctions **321***e* and **321***f* are implanted with an N-type dopant (or a P-type dopant in some implementations) in another separate action. In one implementation, source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* are implanted with an N-type dopant (or a P-type dopant in some implementations) concurrently in a single action. In various implementations, silicide can be situated over source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* and/or gates **324***a*, **324***b*, **324***c*, and **324***d*. In various implementations, semiconductor structure **348** can include more or fewer transistors in crystalline epitaxial layers **358***a*, **358***b*, and **358***c*. For example, another transistor (not shown) can be situated in crystalline epitaxial layer **358***c*, separated from transistors **318***a*, **318***b*, and **318***c* by electrical isolation region **361**. In various implementations, crystalline epitaxial layers **358***a*, **358***b*, **358***c* can include other types of semiconductor devices instead of or in addition to transistors **318***a*, **318***b*, **318***c*, and **304**, such as diodes.

Because semiconductor structure **348** includes porous silicon segment **354**, semiconductor structure **348** reduces RF signal leakage from transistors **318***a*, **318***b*, and **318***c* to ground. Further, porous silicon segment **354** reduces RF signal interference between the different devices built in crystalline epitaxial layers **358***a*, **358***b*, and **358***c*. Pores in porous silicon segment **354** decrease its effective dielectric constant and increase its resistivity. In semiconductor structure **348** in FIG. 3E, porous silicon segment **354** has a dielectric constant significantly less than the dielectric constant of bulk silicon substrate **352**. For example, bulk silicon substrate **352** may have a dielectric constant of approximately 11.7, and porous silicon segment **354** may have a dielectric constant significantly less than 11.7. In particular, porous silicon segment **354** can have a dielectric constant from approximately 2.0 to approximately 4.0.

In semiconductor structure **348** in FIG. 3E, utilizing porous silicon segment **354**, with its low dielectric constant, reduces parasitic capacitance between crystalline epitaxial layer **358***a* and bulk silicon substrate **352**. Accordingly, RF signals are less likely to leak from transistors **318***a*, **318***b*, and **318***c* in crystalline epitaxial layer **358***a* to bulk silicon substrate **352**. For example, in one implementation, transistors **318***a*, **318***b*, and **318***c* are utilized to maintain RF switch **112** (shown in FIG. **1**) in an OFF state, and bulk silicon substrate **352** functions as a ground. In their OFF states, transistors **318***a*, **318***b*, and **318***c* create a high resistance path along source/drain junctions **321***a*, **321***b*, **321***c*, and **321***d*. In this OFF state, the RF signals would have been subject to a significant adverse impact of parasitic capacitances with bulk silicon substrate **352** if porous silicon segment **354** were not utilized. In other words, the RF signals could easily leak from transistors **318***a*, **318***b*, and **318***c* to ground, increasing OFF state parasitic capacitance and negatively impacting the performance of semiconductor structure **348**. Where transistors **318***a*, **318***b*, and **318***c* are transistors utilized to maintain RF switch **112** (shown in FIG. **1**) in an ON state, RF signal leakage, absent porous silicon segment **354**, could also result in a higher insertion loss.

Because semiconductor structure **348** includes porous silicon segment **354** in combination with electrical isolation region **360**, semiconductor structure **348** also reduces RF signal interference from transistor **304** to transistors **318***a*, **318***b*, **318***c*, and vice versa. If porous silicon segment **354** and electrical isolation region **360** were not utilized, RF signals from semiconductor device **304** could propagate through crystalline epitaxial layers **358***b* and **358***a* and/or bulk silicon substrate **352**, and interfere with transistors **318***a*, **318***b*, **318***c* and generate additional undesirable noise in transistors **318***a*, **318***b*, **318***c*. Where transistor **304** is utilized in PA **104** (shown in FIG. **1**) in an RF transmit path, these consequences could be amplified. Similarly, porous silicon segment **354** in combination with electrical isolation region **361** reduces RF signal interference from crystalline epitaxial layer **358***c* to transistors **318***a*, **318***b*, **318***c*, and vice versa. Together, the low dielectric constant of porous silicon segment **354** and electrical insulation of electrical isolation regions **360** and **361** reduce RF signal leakage and interference through crystalline epitaxial layers **358***a*, **358***b*, and **358***c* and/or bulk silicon substrate **352**. The RF signal leakage and interference are especially reduced where depth D1 of electrical isolation regions **360** and **361** is equal to or greater than thickness T1 of crystalline epitaxial layers **358***a*, **358***b*, and **358***c*.

Semiconductor structure **348** in FIG. **3**E can achieve this reduced RF signal leakage without using costly substrate materials, such as quartz or sapphire, and also without requiring costly and/or specialized fabrication techniques used to create trap-rich silicon-on-insulator (SOI) structures, such as smart cut techniques. As described above, porous silicon segment **354** can have a dielectric constant from approximately 2.0 to approximately 4.0, comparable to a buried oxide (BOX) in an SOI structure having a dielectric constant of approximately 3.7. Porous silicon segment **354** can be situated over region **334** of bulk silicon substrate **352**, and included in semiconductor structure **348** by various fabrication techniques. Thereafter, as discussed above, porous silicon segment **354** can be annealed and serve as a high-quality template for growth of crystalline epitaxial layer **358** (shown in FIG. **3**C), in which transistors **318***a*, **318***b*, **318***c*, and **304** are formed.

Because semiconductor structure **348** includes regions **336** and **338** of bulk silicon substrate **352** adjacent to porous silicon segment **354**, semiconductor structure **348** easily accommodates body contacts for transistors, such as transistor **304**. Fewer body contacts can be used in crystalline epitaxial layers **358***b* and **358***c* than in crystalline epitaxial layer **358***a*, since crystalline epitaxial layers **358***b* and **358***c* are situated over regions **336** and **338**, respectively, of bulk silicon substrate **352** having relatively low resistivity compared to porous silicon segment **354** that underlies crystalline epitaxial layer **358***a*. Accordingly, semiconductor structure **348** achieves high device density since in areas outside of RF transistor areas (i.e., outside of crystalline epitaxial layer **358***a*), fewer body contacts are needed.

Further, regions **336** and **338** of bulk silicon substrate **352** adjacent to porous silicon segment **354** increase heat dissipation from crystalline epitaxial layers **358***a* and **358***c*. As described above, in semiconductor structure **348** in FIG. **3**E, regions **336** and **338** of bulk silicon substrate **352** have a thermal conductivity much greater than a BOX in an SOI structure. For example, bulk silicon substrate **352** may have a thermal conductivity of approximately one hundred fifty watts per meter-kelvin (150 W/(m·K)), whereas the BOX may have a thermal conductivity of approximately one and a half watts per meter-kelvin (1.5 W/(m·K)). Accordingly, high power devices, such transistor **304** utilized in PA **104** (shown in FIG. **1**), can be integrated in the same semiconductor structure **348** with transistors **318***a*, **318***b*, and **318***c* without overheating, while also accommodating reduced RF signal leakage. This integration generally reduces losses when connections are ultimately formed between transistor **304** and one of transistors **318***a*, **318***b*, and **318***c*.

FIG. **3**F illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with actions **248***a* and **248***b* in the flowchart of FIG. **2** according to one implementation of the present application. Semiconductor structure **348** of FIG. **3**F represents an alternative implementation to semiconductor structure **348** of FIG. **3**E. Semiconductor structure **348** of FIG. **3**F is similar to semiconductor structure **348** of FIG. **3**E, except that, in semiconductor structure **348** of FIG. **3**F, depth D3 of source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* is substantially equal to thickness T1 of crystalline epitaxial layers **358***a*, **358***b*, and **358***c*, such that source/drain junctions **321***a*, **321***b*, **321***c*, and **321***d* are in contact with porous silicon segment **354**, and such that source/drain junctions **321***e* and **321***f* are in contact with region **336** of bulk silicon substrate **352**. In semiconductor structure **348** of FIG. **3**E, shallow source/drain junctions **321***a*, **321***b*, **321***c*, and **321***d* improve performance of transistors **318***a*, **318***b*, and **318***c* by reducing junction capacitances. In semiconductor structure **348** of FIG. **3**F, deeper source/drain junctions **321***e* and **321***f* improve performance of transistor **304** by improving high current and high voltage handling. Other than the differences described above, semiconductor structure **348** of FIG. **3**F may have any implementations and advantages described above with respect to semiconductor structure **348** of FIG. **3**E.

From the above description it is manifest that various techniques can be used for implementing the concepts described in the present application without departing from the scope of those concepts. Moreover, while the concepts have been described with specific reference to certain implementations, a person of ordinary skill in the art would recognize that changes can be made in form and detail without departing from the scope of those concepts. As such, the described implementations are to be considered in all respects as illustrative and not restrictive. It should also be understood that the present application is not limited to the particular implementations described above, but many rearrangements, modifications, and substitutions are possible without departing from the scope of the present disclosure.

The invention claimed is:

1. A semiconductor structure comprising:

a porous semiconductor segment adjacent to a first region of a substrate;

at least one crystalline epitaxial layer situated over said porous semiconductor segment and over said first region of said substrate;

a first semiconductor device situated in said at least one crystalline epitaxial layer over said porous semiconductor segment;

a second semiconductor device situated in said at least one crystalline epitaxial layer over said first region of said substrate but not over said porous semiconductor segment;

said first region of said substrate having a first dielectric constant, and said porous semiconductor segment having a second dielectric constant that is substantially less than said first dielectric constant such that said porous semiconductor segment reduces signal leakage from said first semiconductor device.

2. The semiconductor structure of claim **1**, wherein a second region of said substrate is situated under said porous semiconductor segment and under said first region of said substrate.

3. The semiconductor structure of claim **1**, further comprising:

an electrical isolation region separating said first and second semiconductor devices.

4. The semiconductor structure of claim **3**, wherein a depth of said electrical isolation region is equal to or greater than a thickness of said at least one crystalline epitaxial layer.

5. The semiconductor structure of claim **1**, wherein said first semiconductor device is a transistor utilized in a radio frequency (RF) switch.

6. The semiconductor structure of claim **5**, wherein a depth of a source/drain junction of said transistor is substantially less than a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is not in contact with said porous semiconductor segment.

7. The semiconductor structure of claim **5**, wherein a depth of a source/drain junction of said transistor is substantially equal to a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is in contact with said porous semiconductor segment.

8. A semiconductor structure comprising:

a porous silicon segment adjacent to a first region of a bulk silicon substrate;

at least one crystalline epitaxial layer situated over said porous silicon segment and over said first region of said bulk silicon substrate;

a first transistor situated in said at least one crystalline epitaxial layer over said porous silicon segment;

a second transistor situated in said at least one crystalline epitaxial layer over said first region of said bulk silicon substrate but not over said porous silicon segment;

an electrical isolation region separating said first and second transistors.

9. The semiconductor structure of claim 8, wherein a second region of said bulk silicon substrate is situated under said porous silicon segment and under said first region of said bulk silicon substrate.

10. The semiconductor structure of claim 8, wherein a depth of said electrical isolation region is equal to or greater than a thickness of said at least one crystalline epitaxial layer.

11. The semiconductor structure of claim 8, wherein said first transistor is utilized in a radio frequency (RF) switch.

12. The semiconductor structure of claim 8, wherein a depth of a source/drain junction of said first transistor is substantially less than a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is not in contact with said porous silicon segment.

13. The semiconductor structure of claim 8, wherein a depth of a source/drain junction of said first transistor is substantially equal to a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is in contact with said porous silicon segment.

14. A semiconductor structure comprising:

a porous silicon segment adjacent to a bulk silicon substrate;

at least one crystalline epitaxial layer having a first region situated over said porous silicon segment;

said at least one crystalline epitaxial layer having a second region situated over said bulk silicon substrate but not over said porous silicon segment;

an electrical isolation region separating said first region of said at least one crystalline epitaxial layer from said second region of said at least one crystalline epitaxial layer.

15. The semiconductor structure of claim 14, wherein a depth of said electrical isolation region is equal to or greater than a thickness of said at least one crystalline epitaxial layer.

16. The semiconductor structure of claim 14, wherein a first semiconductor device is situated in said first region of said at least one crystalline epitaxial layer and a second semiconductor device is situated in said second region of said at least one crystalline epitaxial layer.

17. The semiconductor structure of claim 16, wherein said first semiconductor device is a first transistor and wherein a depth of a source/drain junction of said first transistor is substantially less than a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is not in contact with said porous silicon segment.

18. The semiconductor structure of claim 16, wherein said first semiconductor device is a first transistor and wherein a depth of a source/drain junction of said first transistor is substantially equal to a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is in contact with said porous silicon segment.

19. The semiconductor structure of claim 16, wherein said first semiconductor device is a first transistor that is utilized in a radio frequency (RF) switch.

* * * * *

Exhibit 4

US011145572B2

(12) **United States Patent**
Howard

(10) **Patent No.: US 11,145,572 B2**
(45) **Date of Patent: Oct. 12, 2021**

(54) **SEMICONDUCTOR STRUCTURE HAVING THROUGH-SUBSTRATE VIA (TSV) IN POROUS SEMICONDUCTOR REGION**

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(72) Inventor: **David J. Howard**, Irvine, CA (US)

(73) Assignee: **Newport Fab, LLC**, Newport Beach, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **16/703,367**

(22) Filed: **Dec. 4, 2019**

(65) **Prior Publication Data**

US 2021/0111101 A1 Apr. 15, 2021

Related U.S. Application Data

(63) Continuation-in-part of application No. 16/598,803, filed on Oct. 10, 2019, and a continuation-in-part of application No. 16/597,779, filed on Oct. 9, 2019.

(51) **Int. Cl.**

H01L 23/48	(2006.01)
H01L 23/00	(2006.01)
H01L 21/768	(2006.01)
H01L 23/373	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 23/481*** (2013.01); ***H01L 21/76831*** (2013.01); ***H01L 21/76898*** (2013.01); ***H01L 23/3733*** (2013.01); ***H01L 23/562*** (2013.01)

(58) **Field of Classification Search**

CPC . H01L 23/481; H01L 23/562; H01L 23/3733; H01L 23/48; H01L 23/00; H01L 23/373; H01L 21/768; H01L 21/76831; H01L 21/76898

USPC 257/728

See application file for complete search history.

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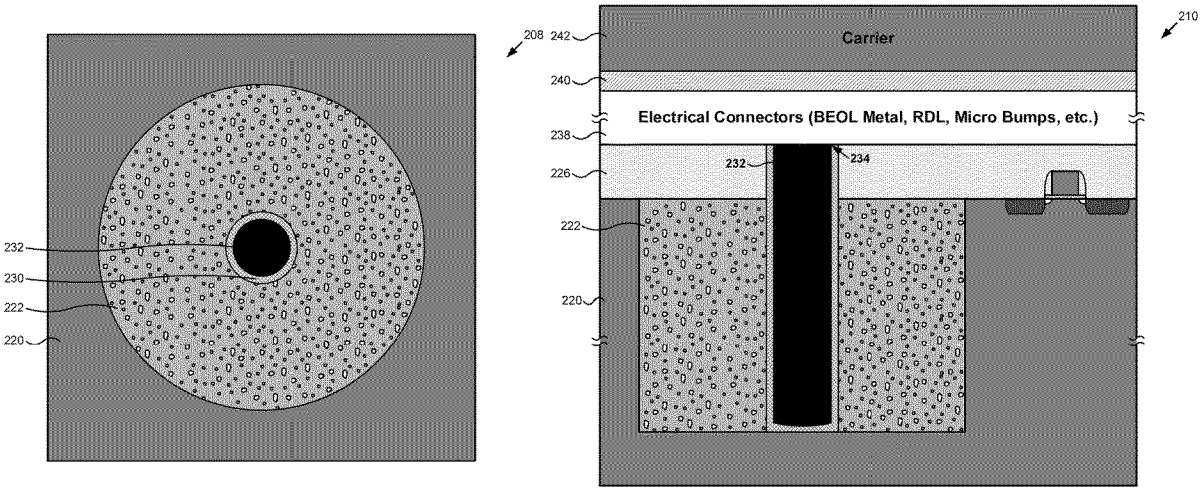
Primary Examiner — Alexander O Williams

(74) *Attorney, Agent, or Firm* — Farjami & Farjami LLP

(57) **ABSTRACT**

A semiconductor structure includes a semiconductor substrate, a porous semiconductor region within the semiconductor substrate, and through-substrate via (TSV) within the porous semiconductor region. The porous semiconductor region causes the semiconductor structure and/or the TSV to withstand thermal and mechanical stresses. Alternatively, the semiconductor structure includes a semiconductor buffer ring within the porous semiconductor region, and the TSV within the semiconductor buffer ring.

21 Claims, 25 Drawing Sheets



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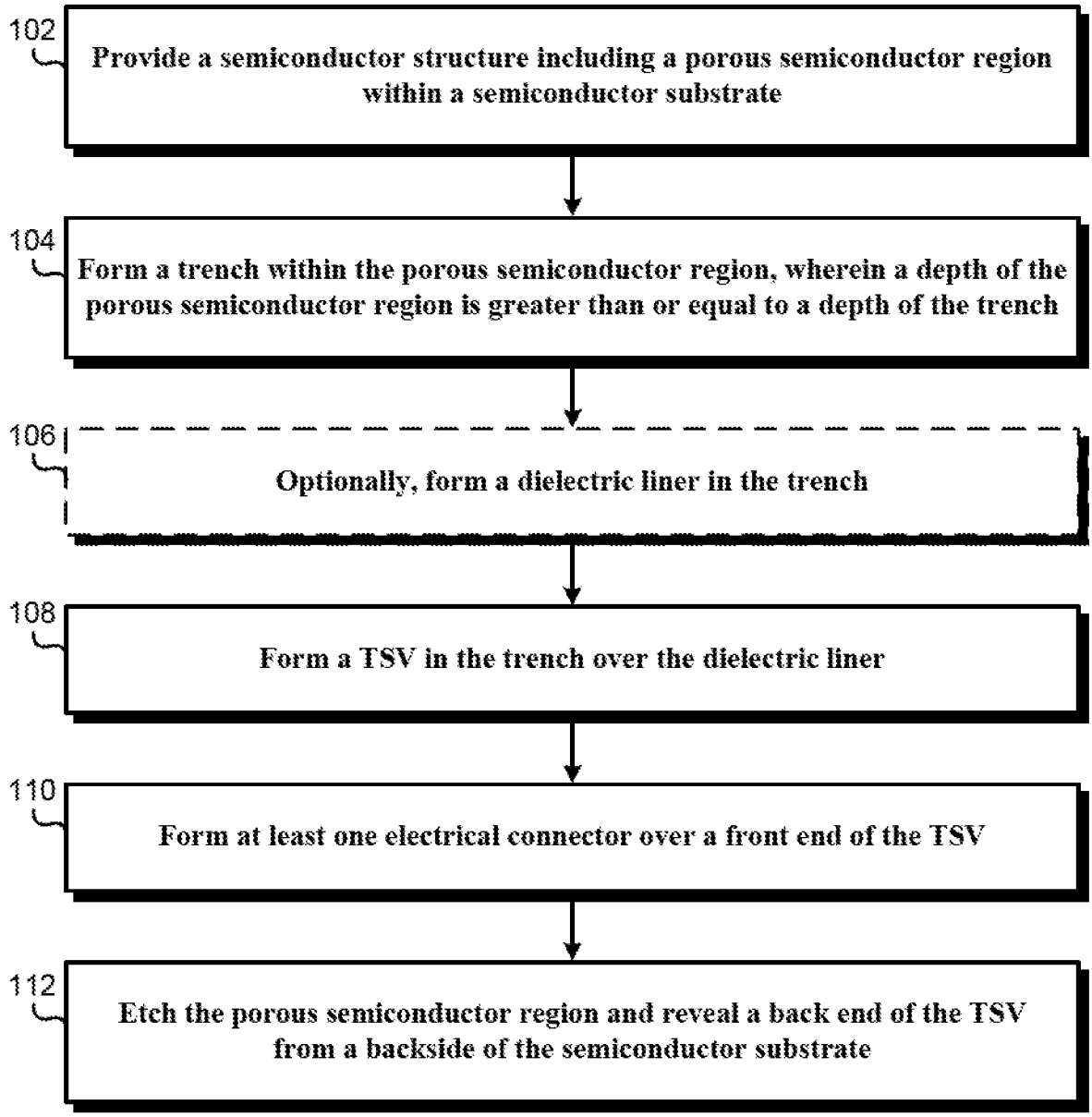

102
Provide a semiconductor structure including a porous semiconductor region within a semiconductor substrate
104
Form a trench within the porous semiconductor region, wherein a depth of the porous semiconductor region is greater than or equal to a depth of the trench
106
Optionally, form a dielectric liner in the trench
108
Form a TSV in the trench over the dielectric liner
110
Form at least one electrical connector over a front end of the TSV
112
Etch the porous semiconductor region and reveal a back end of the TSV from a backside of the semiconductor substrate

FIG. 1

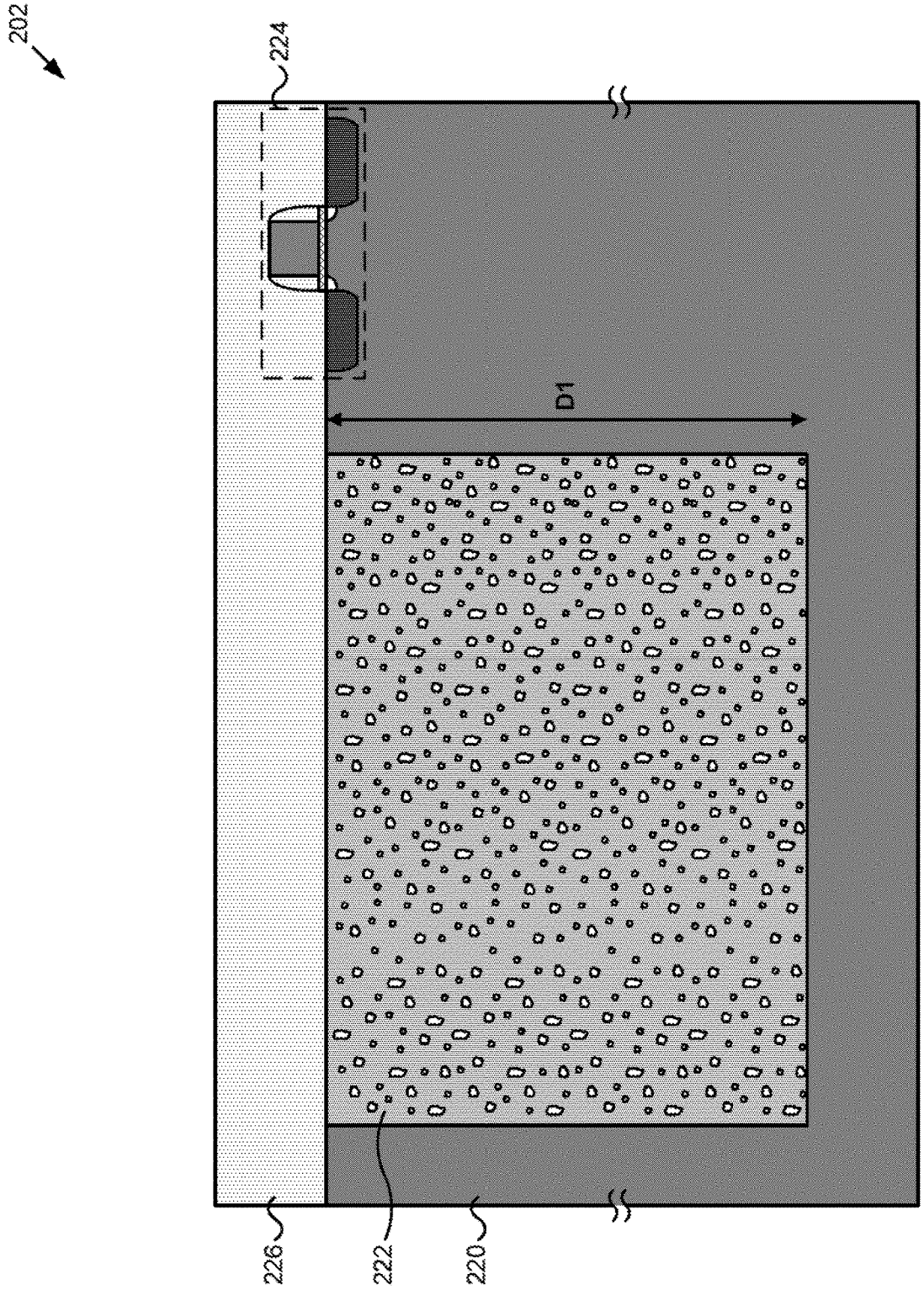


FIG. 2A

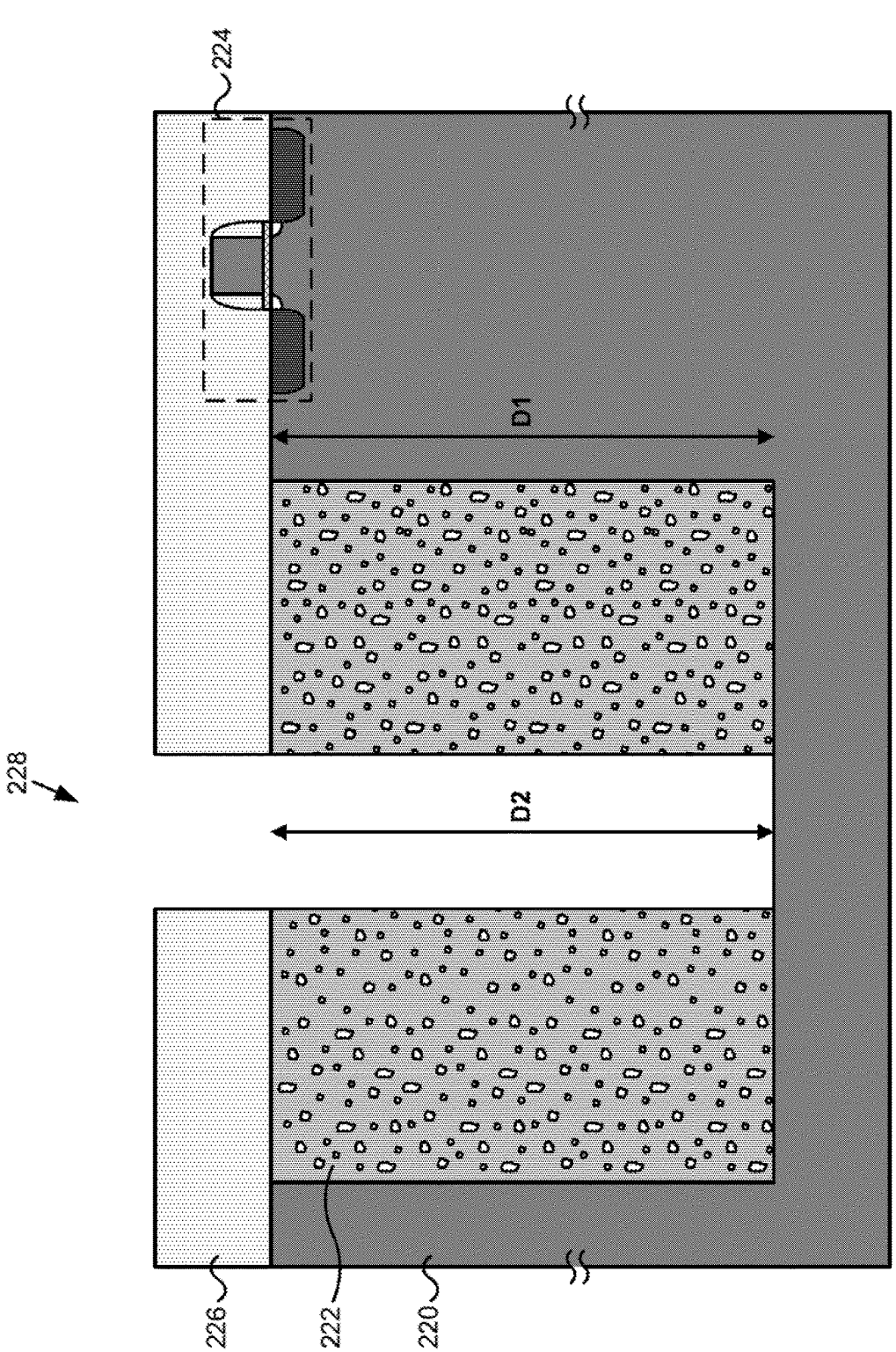


FIG. 2B

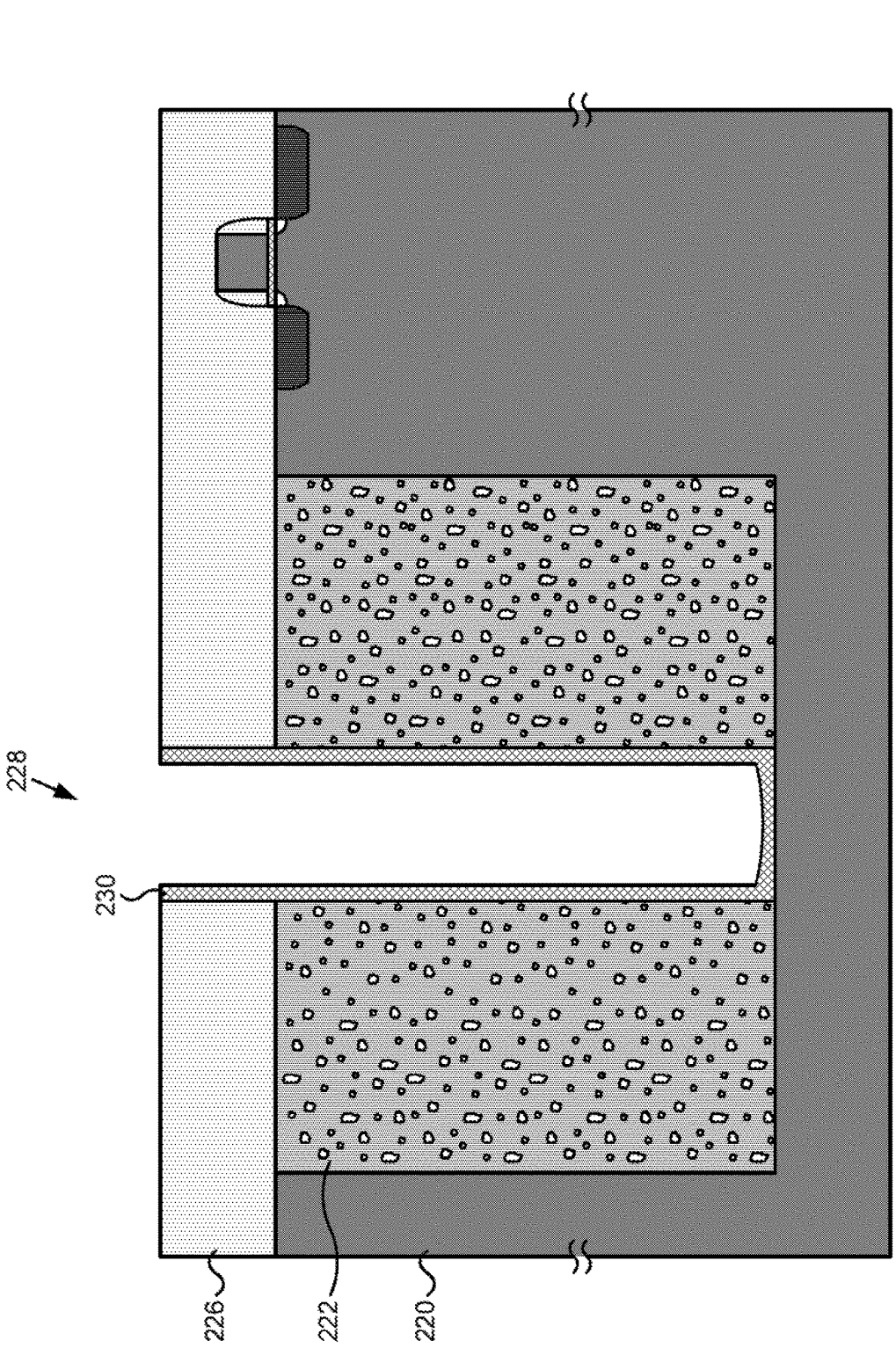


FIG. 2C

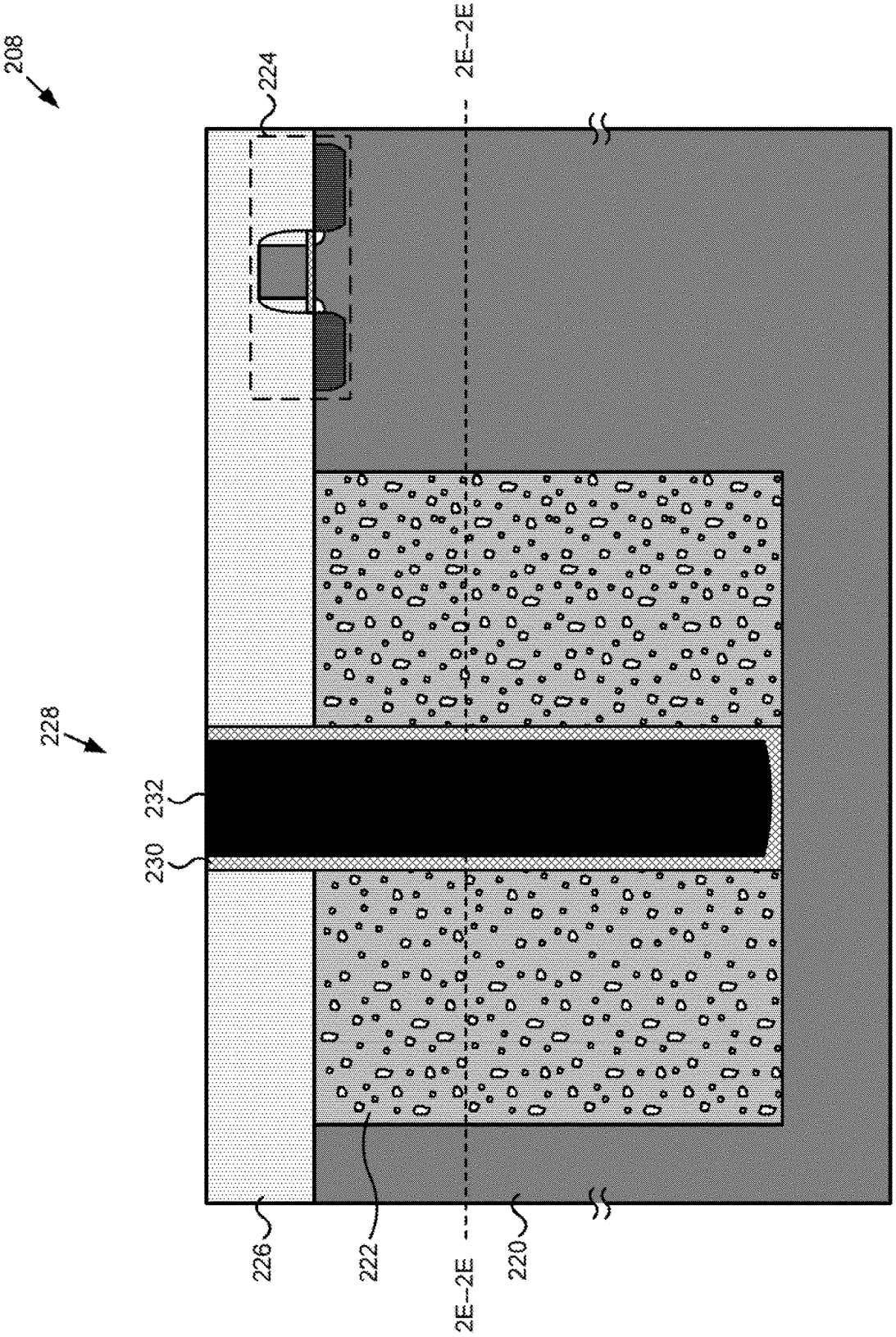


FIG. 2D

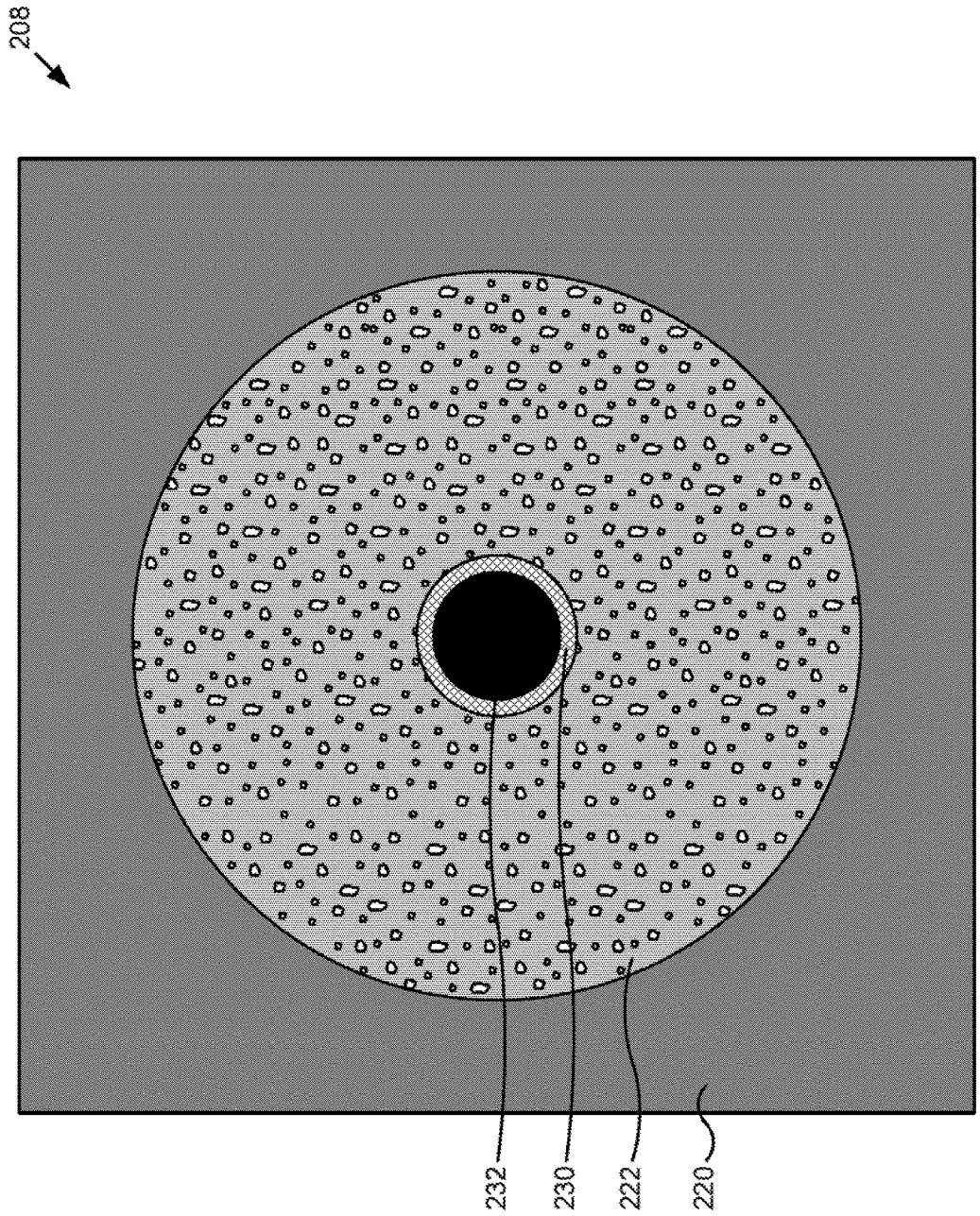


FIG. 2E

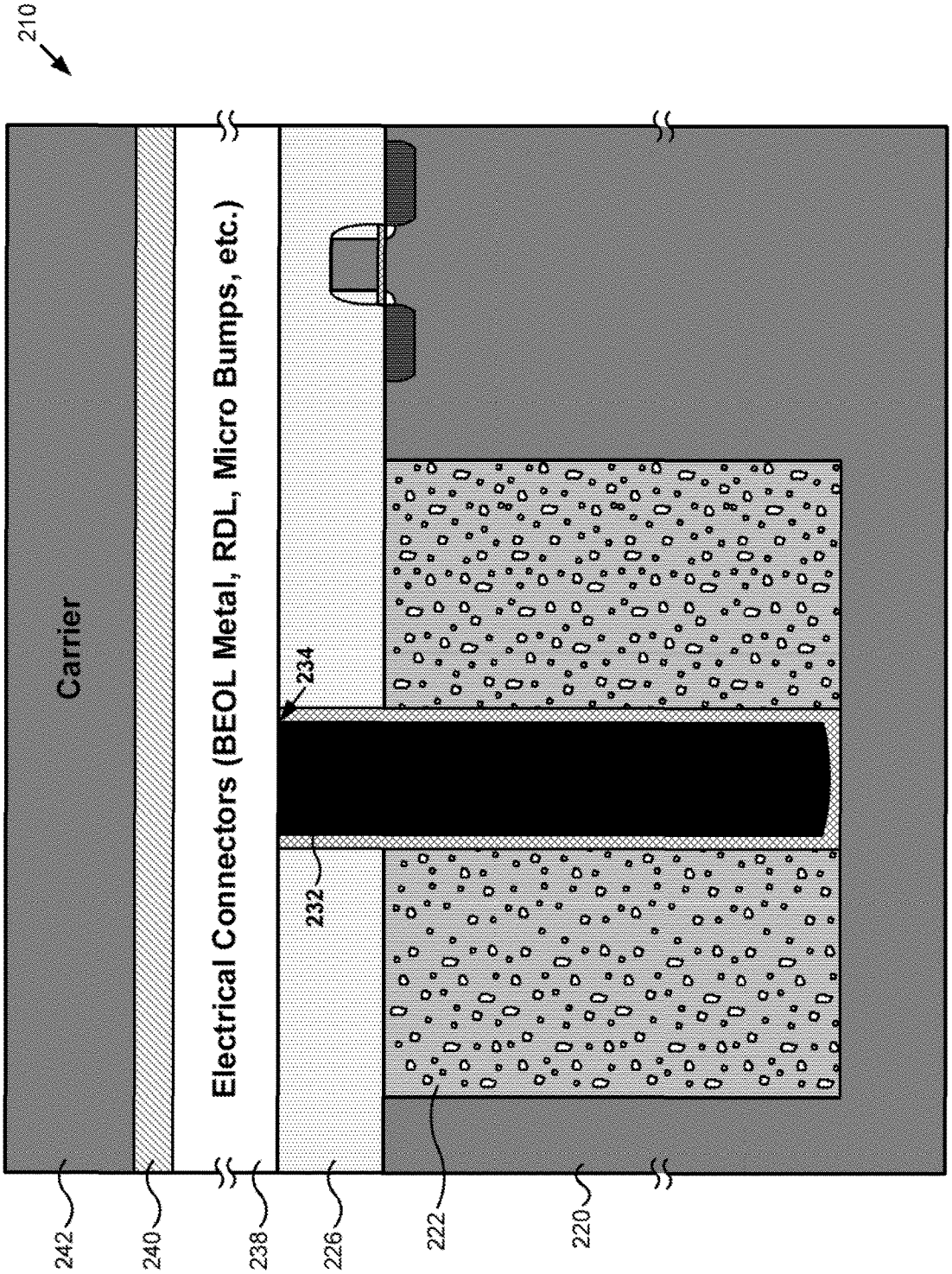
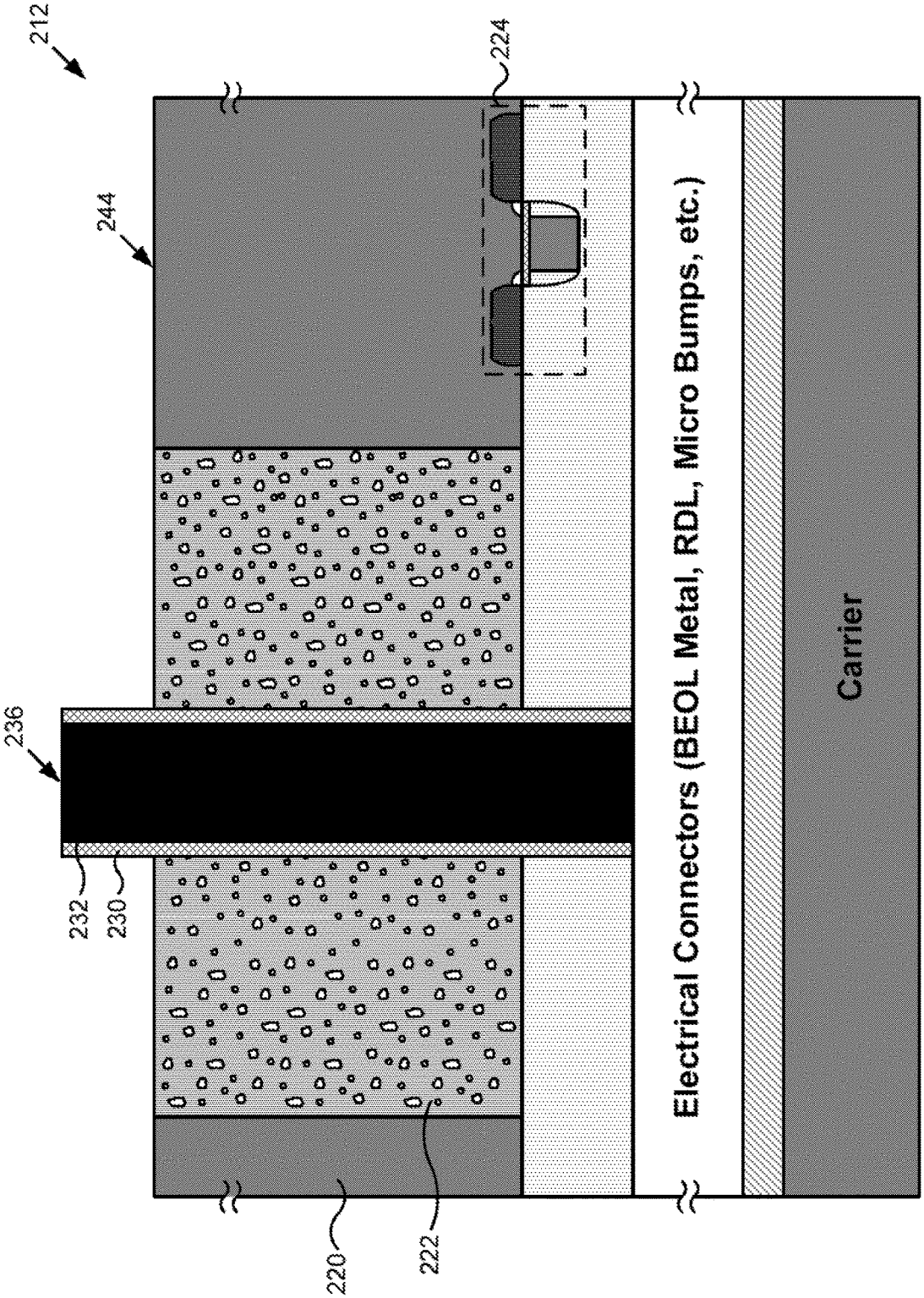

210
Carrier
Electrical Connectors (BEOL Metal, RDL, Micro Bumps, etc.)
234
232
242
240
238
226
222
220

FIG. 2F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224
244
236
232
230
220
222
Electrical Connectors (BEOL Metal, RDL, Micro Bumps, etc.)
Carrier

FIG. 2G

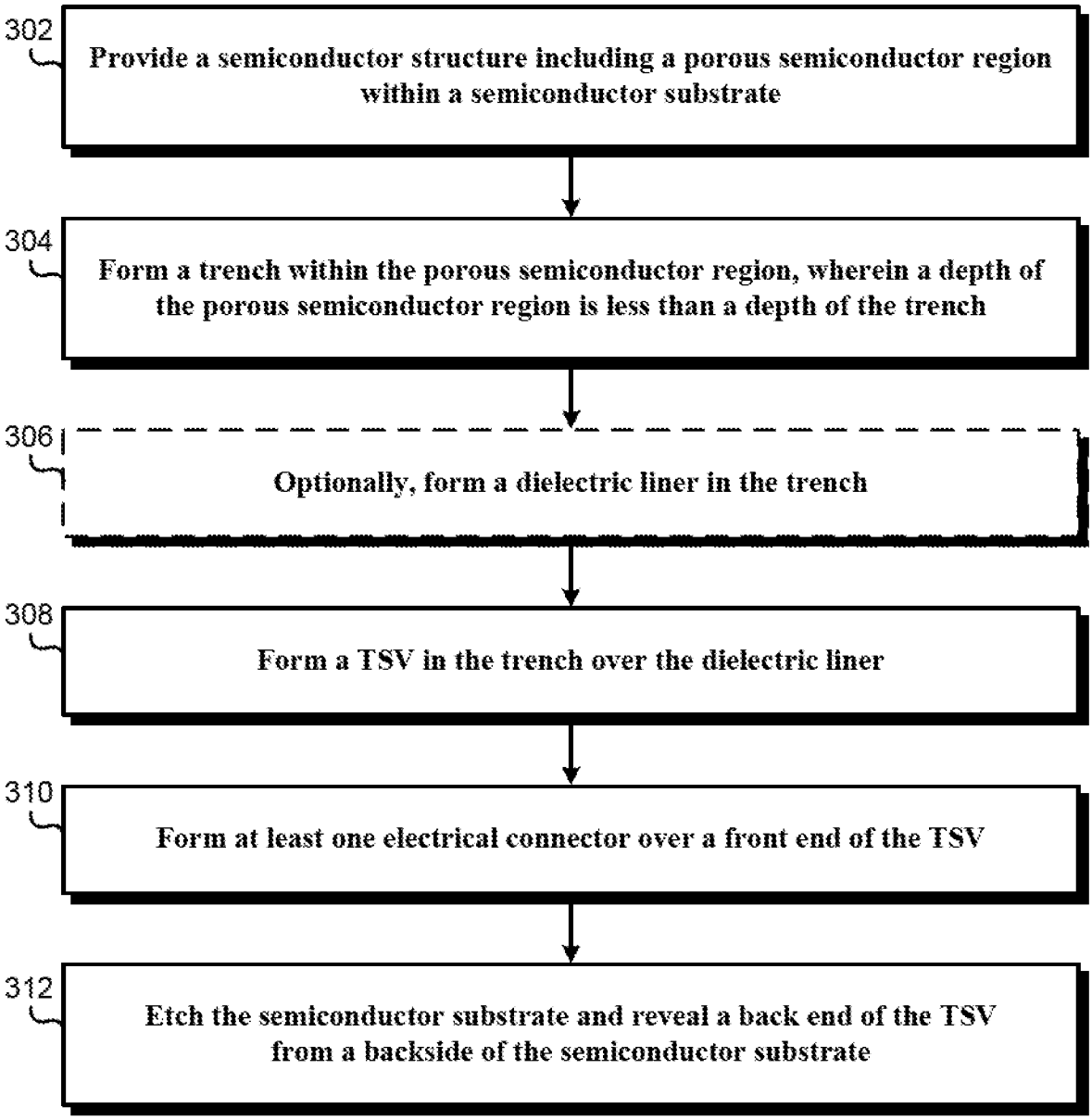
302
Provide a semiconductor structure including a porous semiconductor region within a semiconductor substrate
304
Form a trench within the porous semiconductor region, wherein a depth of the porous semiconductor region is less than a depth of the trench
306
Optionally, form a dielectric liner in the trench
308
Form a TSV in the trench over the dielectric liner
310
Form at least one electrical connector over a front end of the TSV
312
Etch the semiconductor substrate and reveal a back end of the TSV from a backside of the semiconductor substrate

FIG. 3

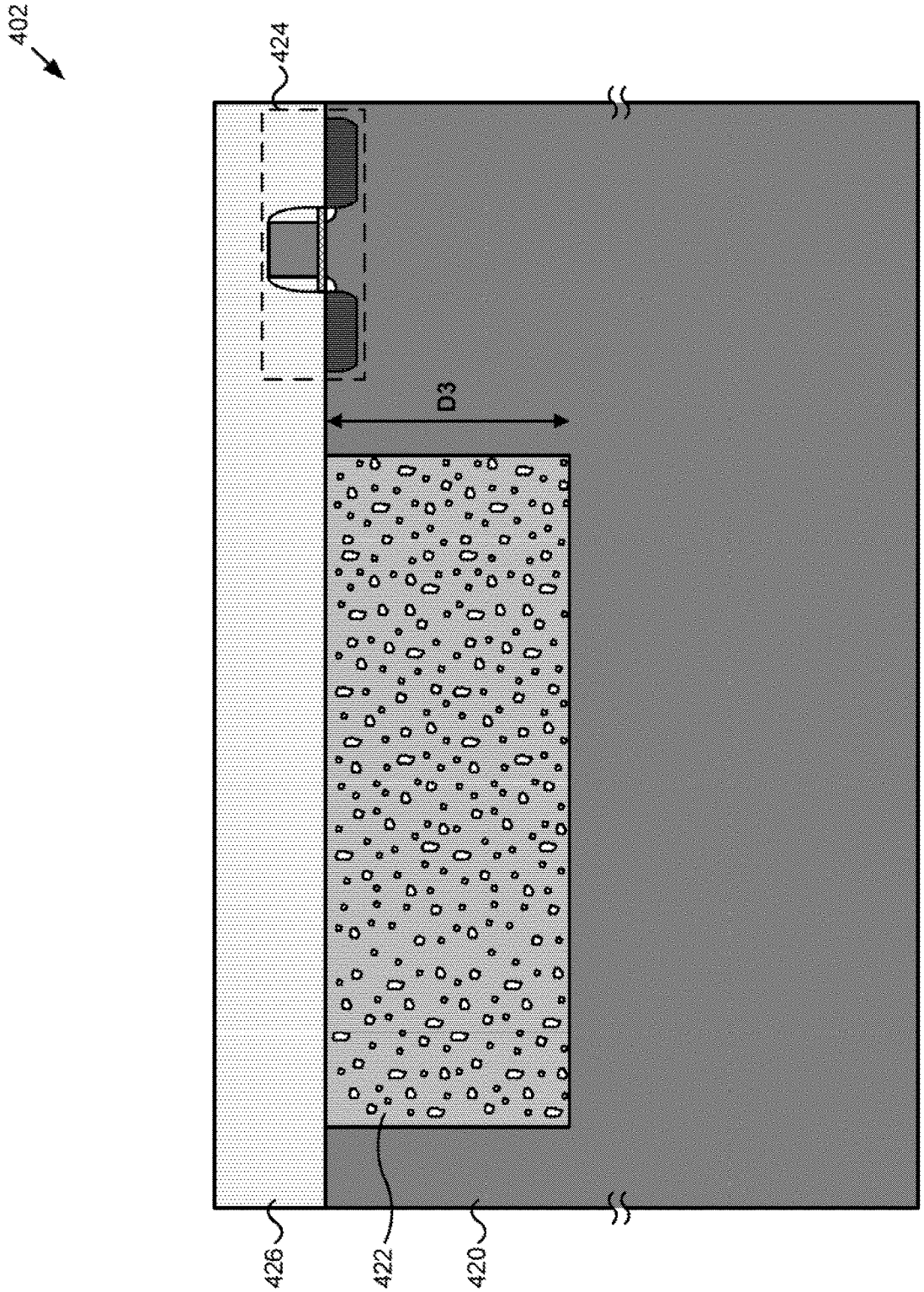

FIG. 4A

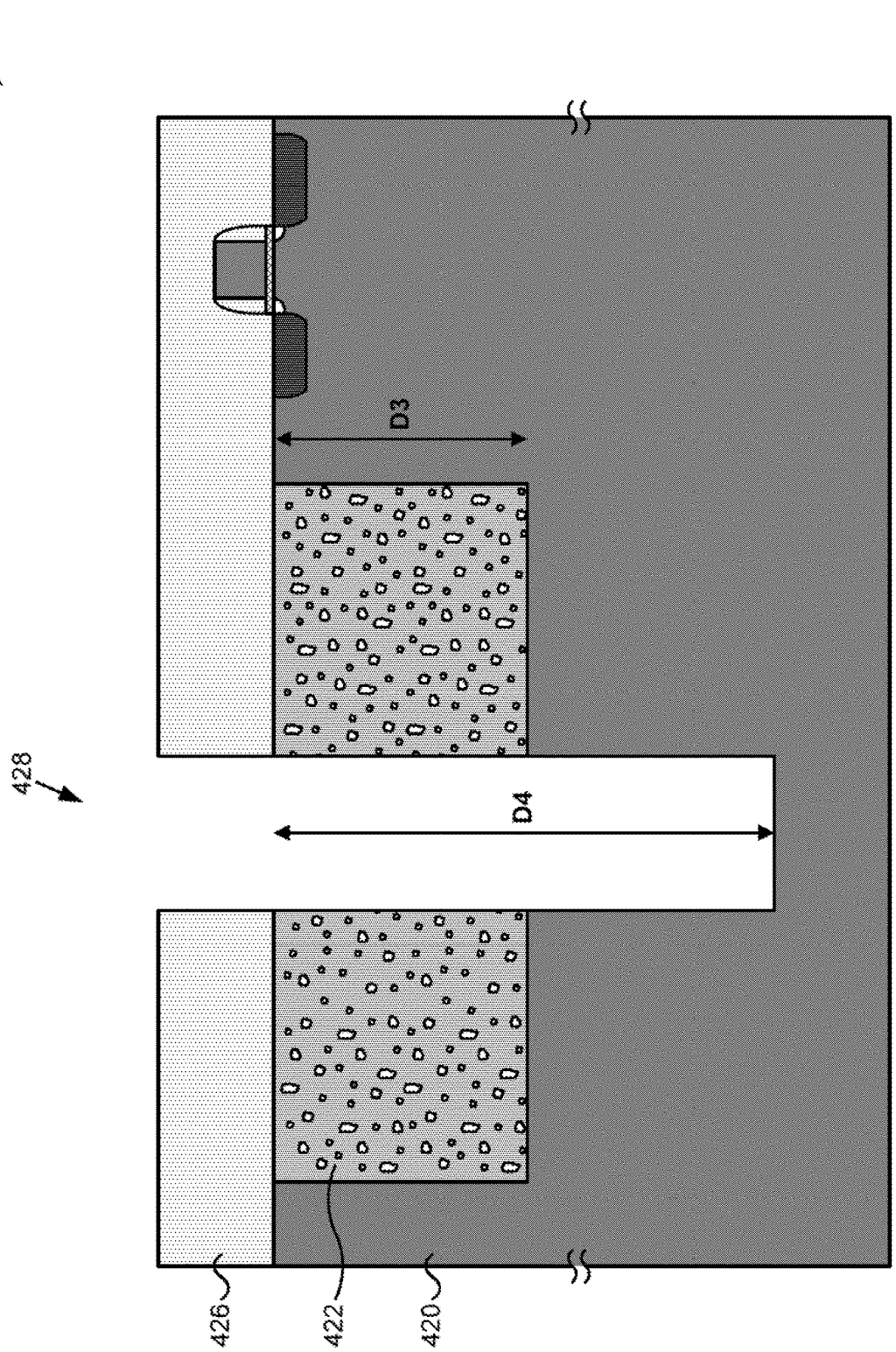

FIG. 4B

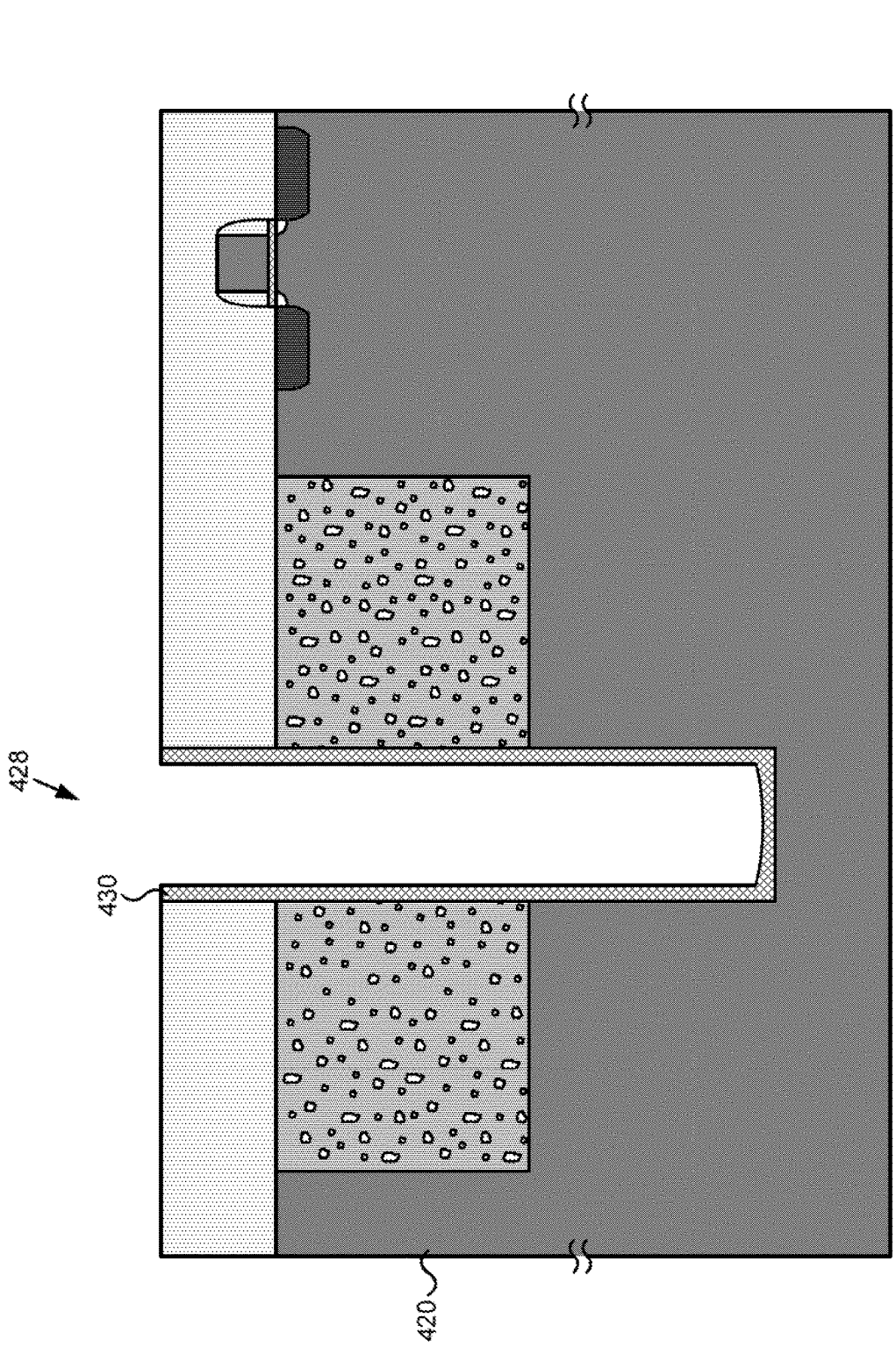

FIG. 4C

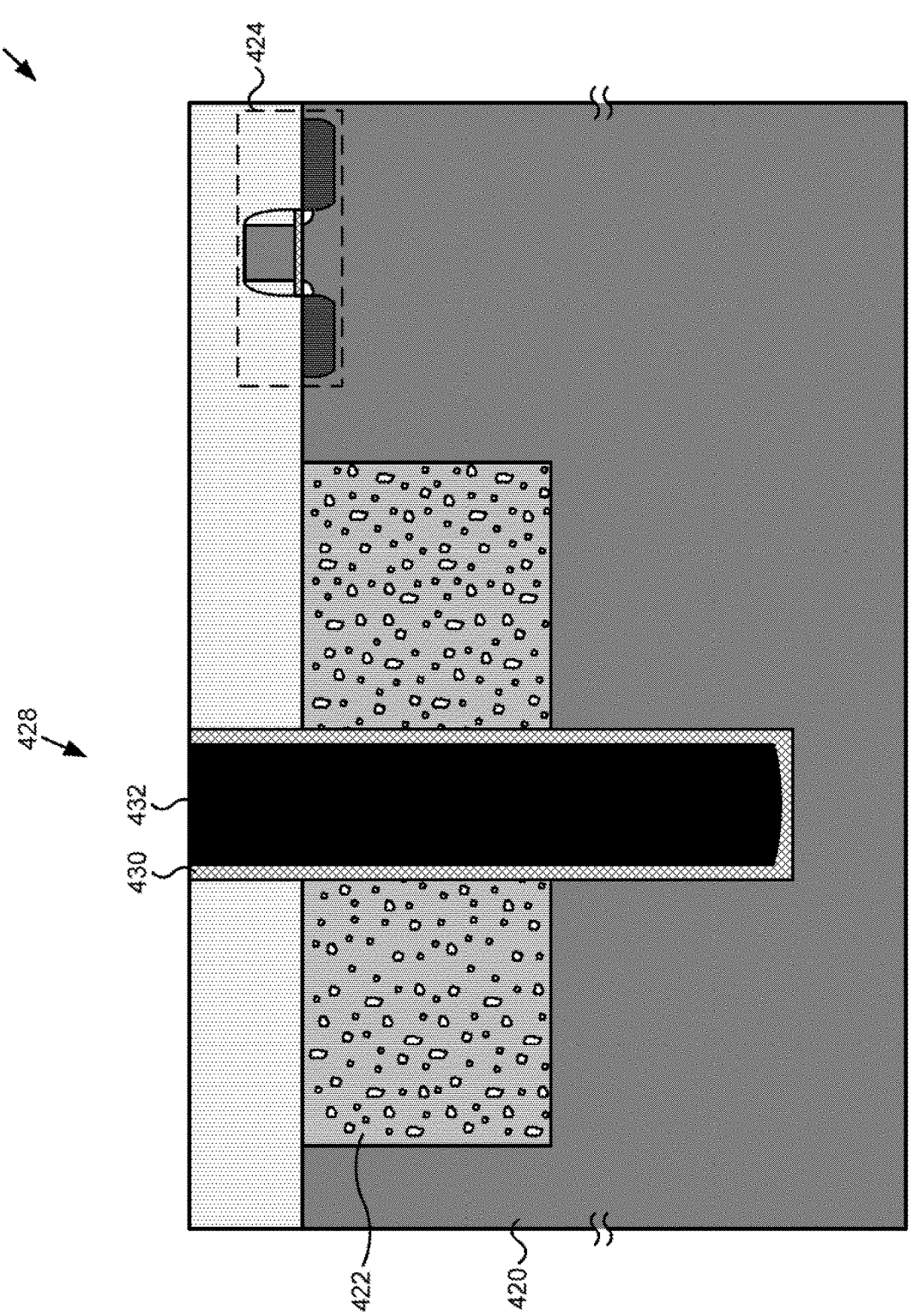

FIG. 4D

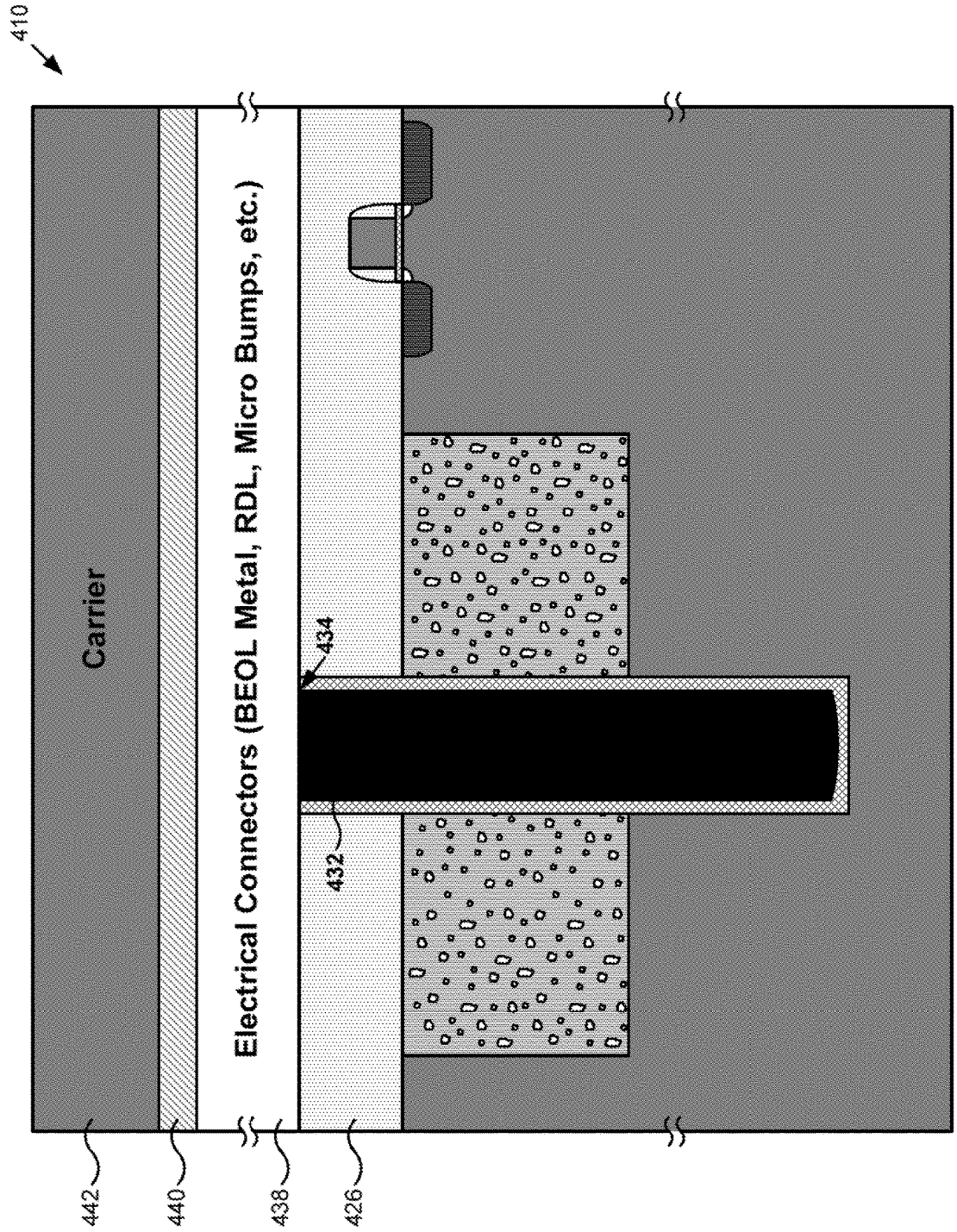
410
Carrier
Electrical Connectors (BEOL Metal, RDL, Micro Bumps, etc.)
434
432
442
440
438
426

FIG. 4E

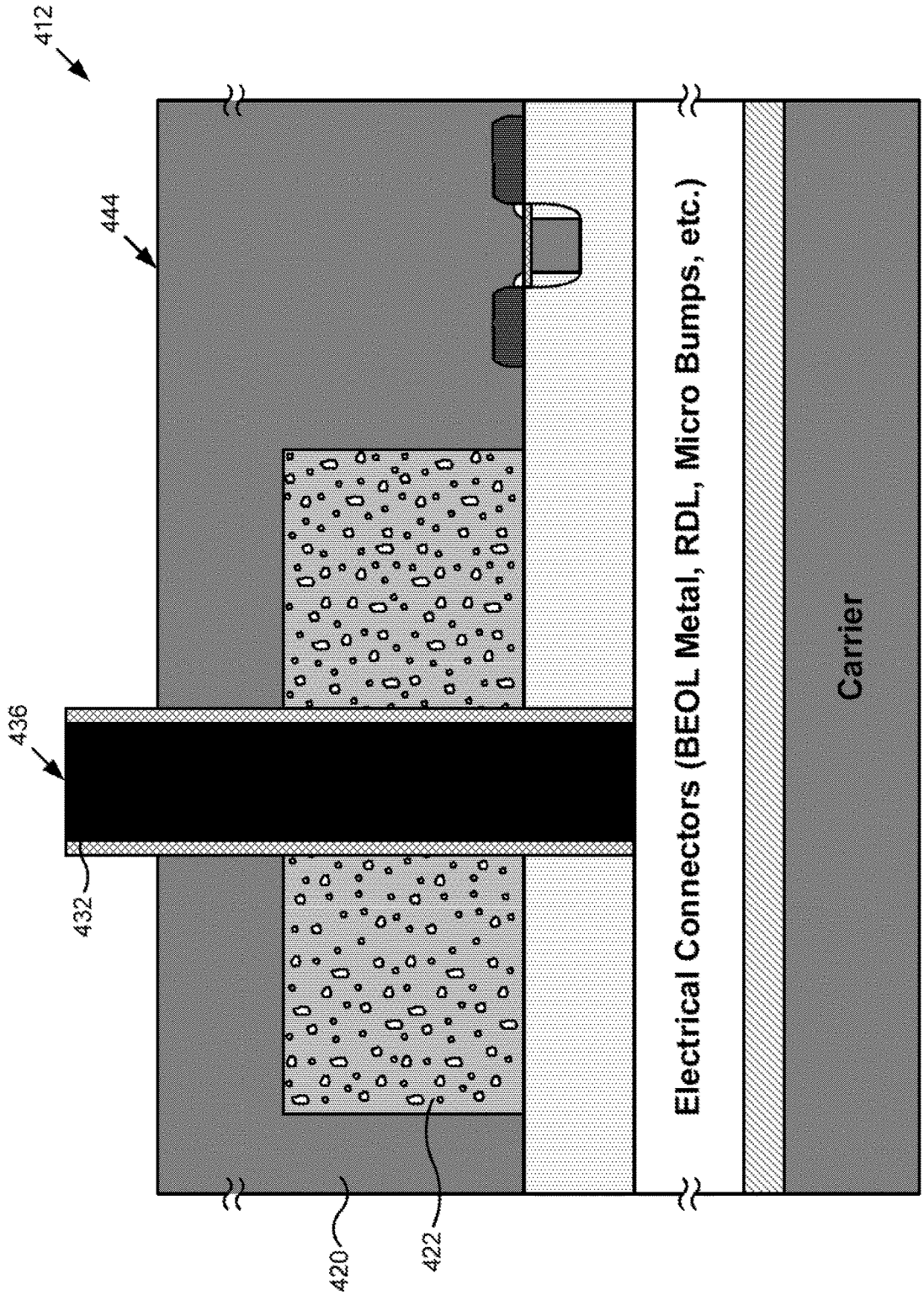
412
444
436
432
420
422
Electrical Connectors (BEOL Metal, RDL, Micro Bumps, etc.)
Carrier

FIG. 4F

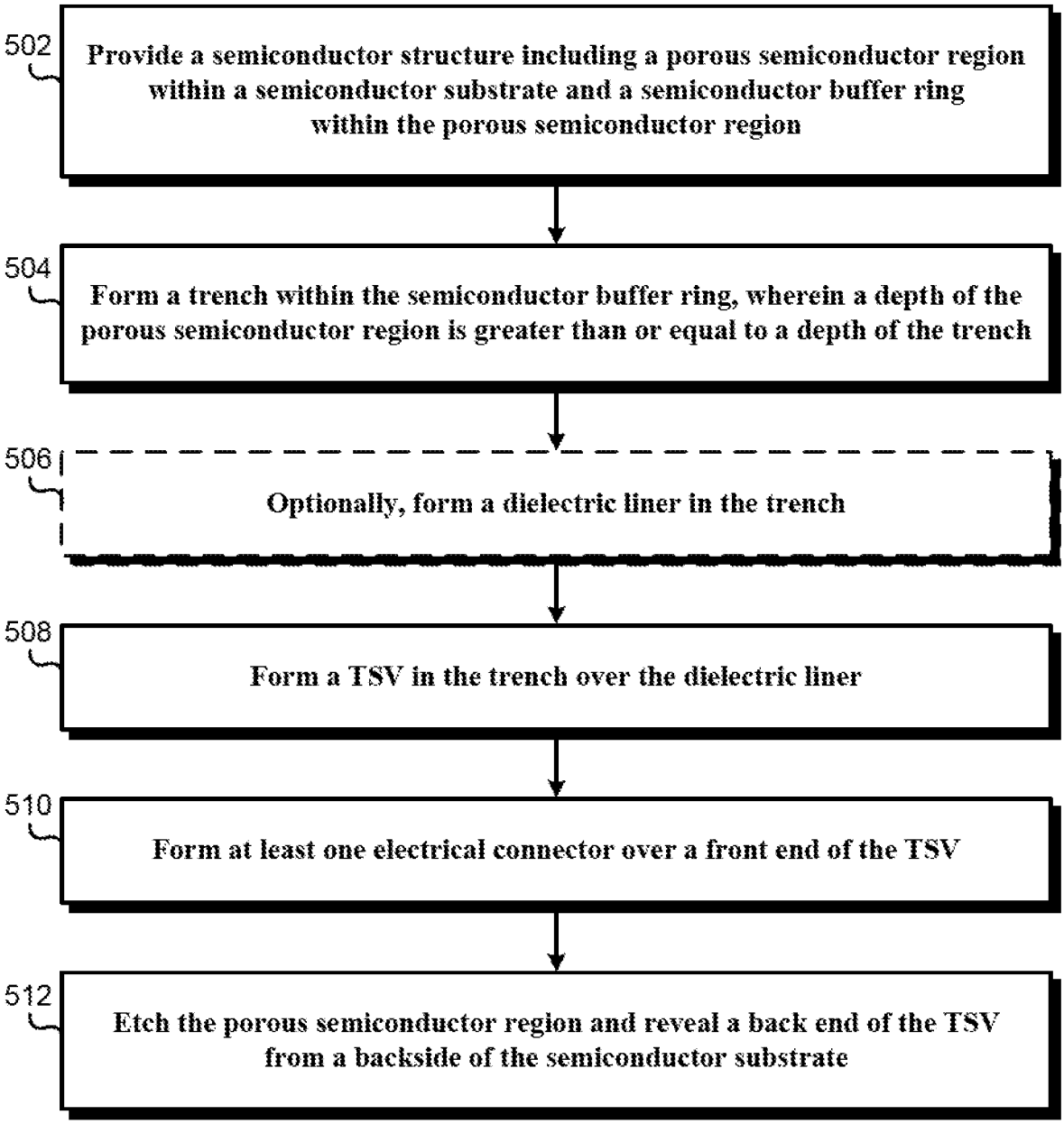
502
Provide a semiconductor structure including a porous semiconductor region within a semiconductor substrate and a semiconductor buffer ring within the porous semiconductor region
504
Form a trench within the semiconductor buffer ring, wherein a depth of the porous semiconductor region is greater than or equal to a depth of the trench
506
Optionally, form a dielectric liner in the trench
508
Form a TSV in the trench over the dielectric liner
510
Form at least one electrical connector over a front end of the TSV
512
Etch the porous semiconductor region and reveal a back end of the TSV from a backside of the semiconductor substrate

FIG. 5

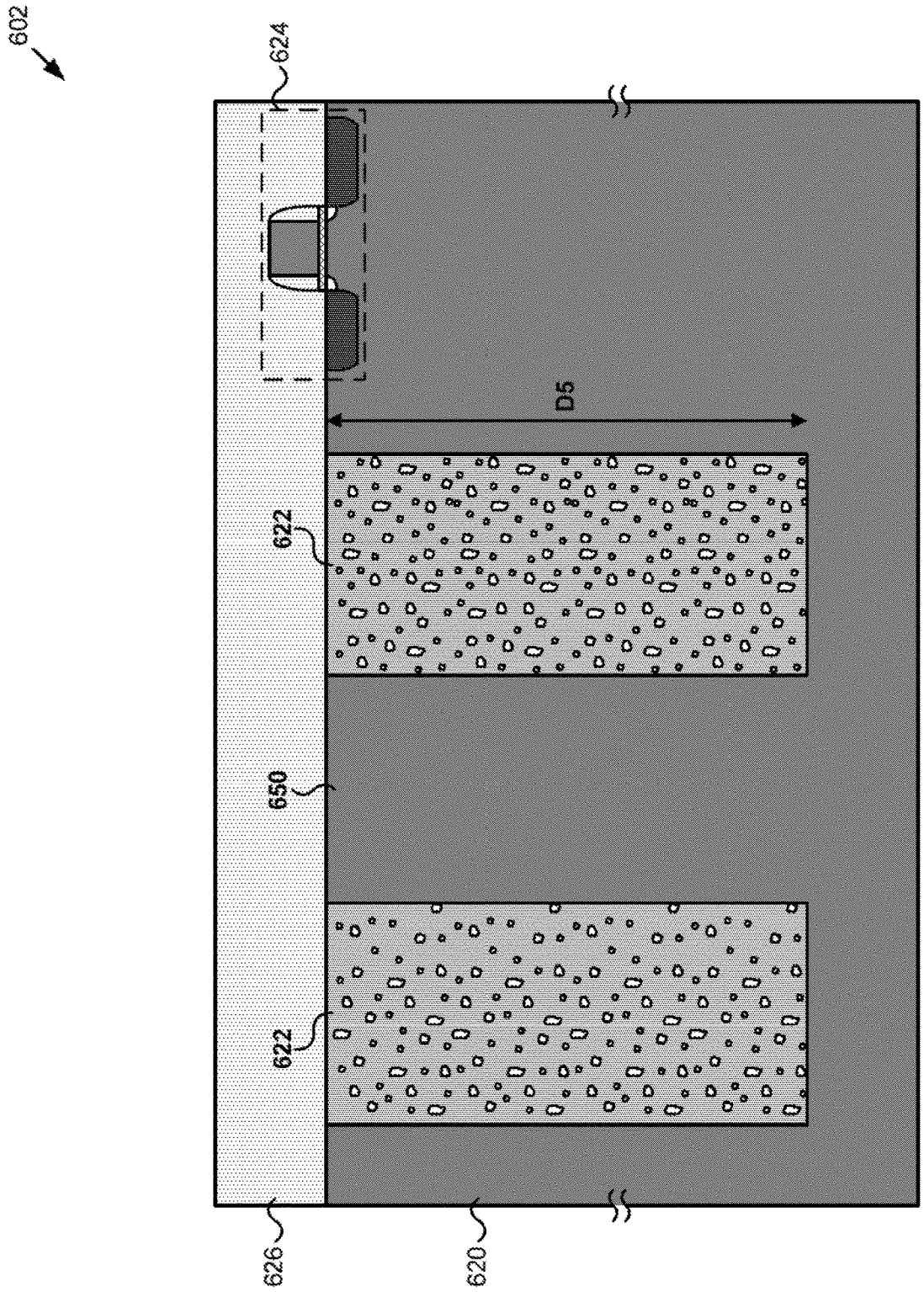

FIG. 6A

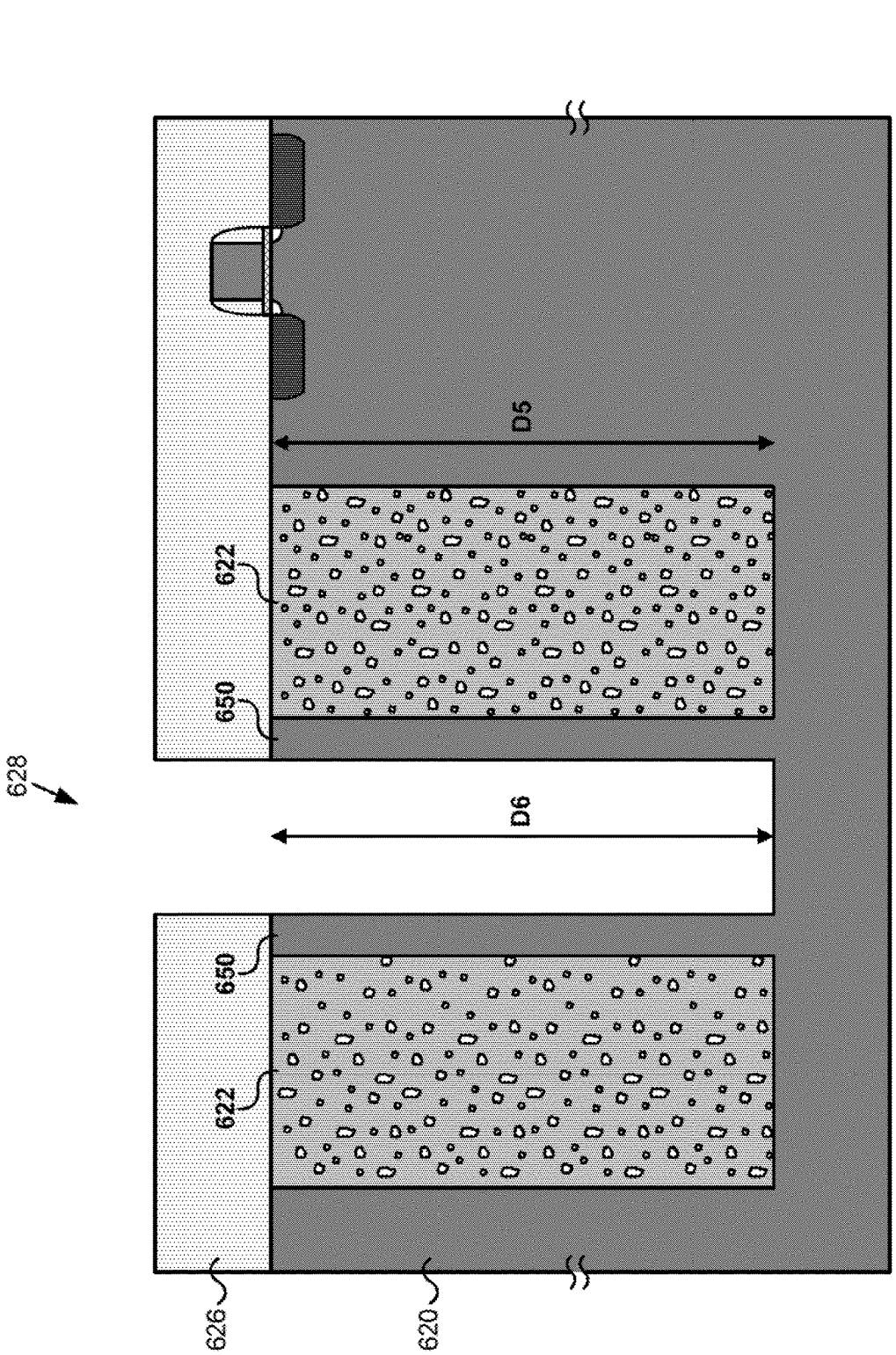

FIG. 6B

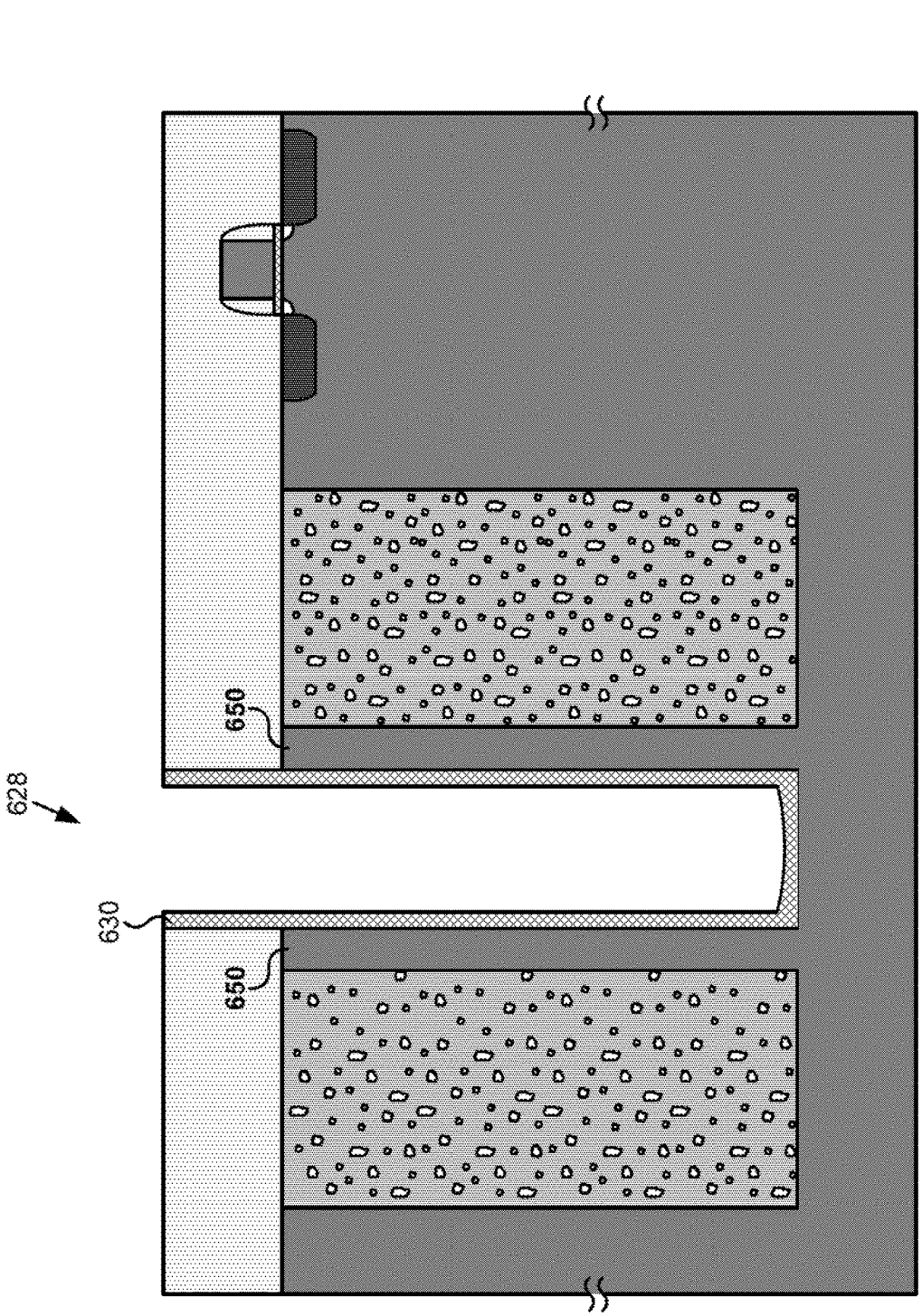

FIG. 6C

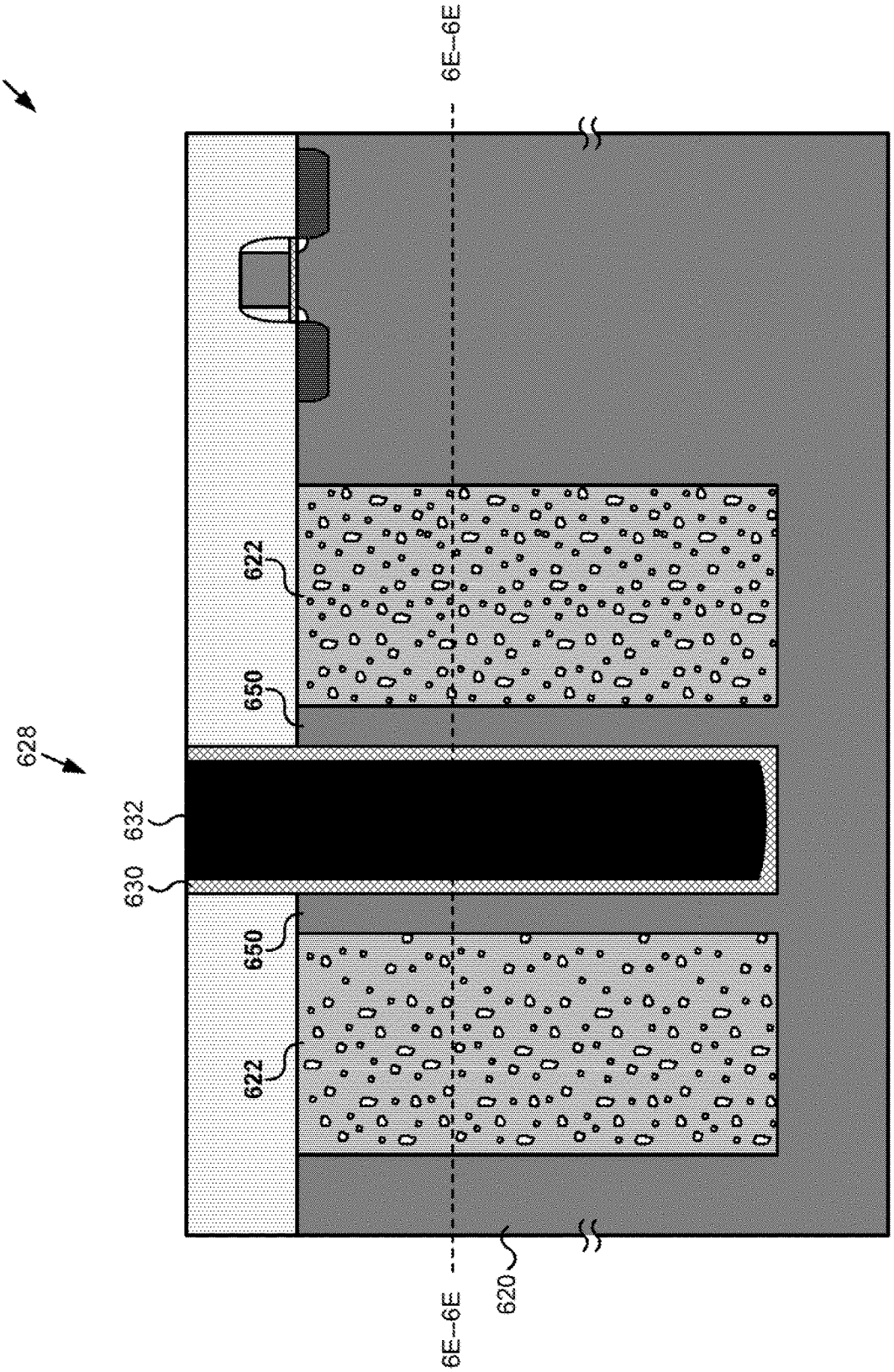

FIG. 6D

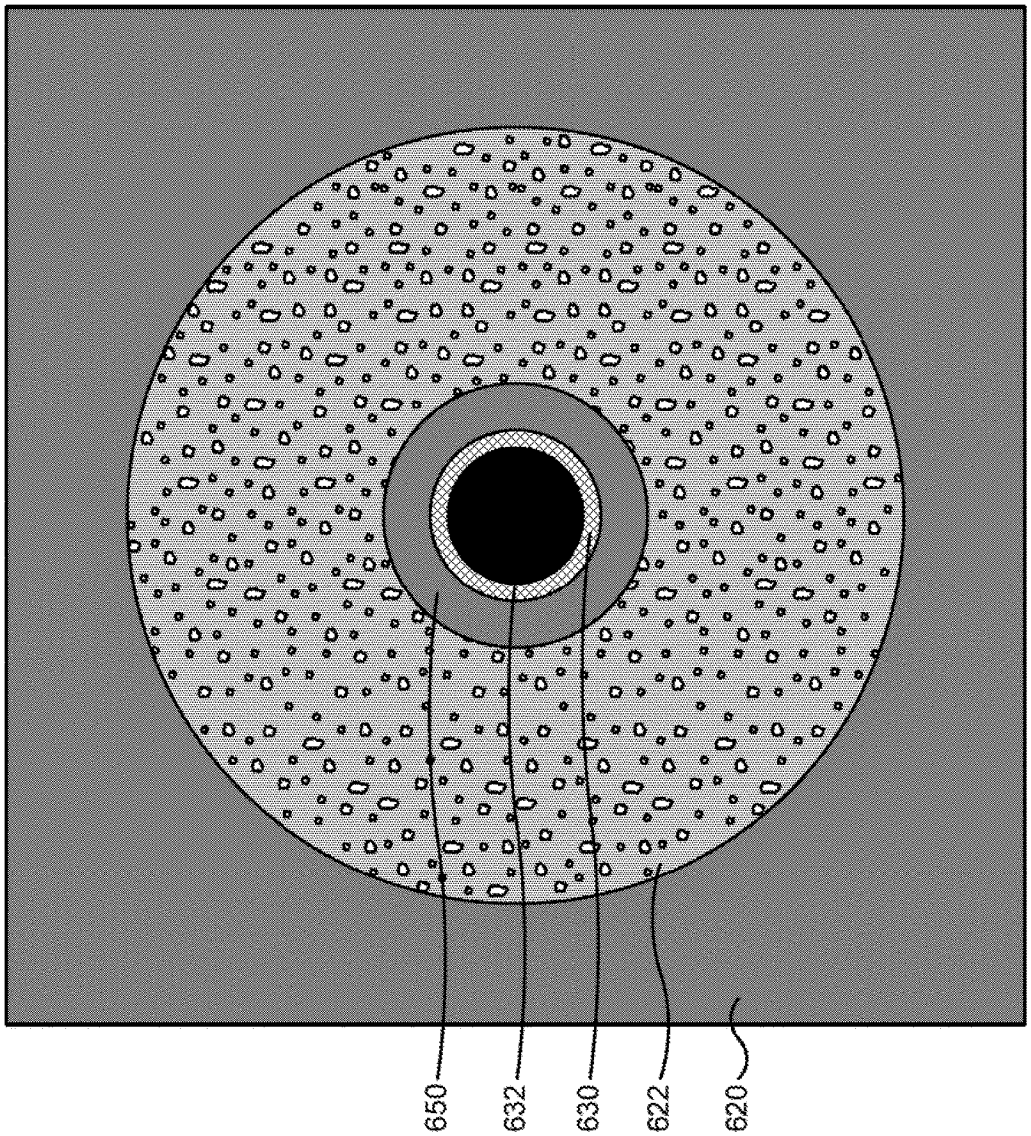

FIG. 6E

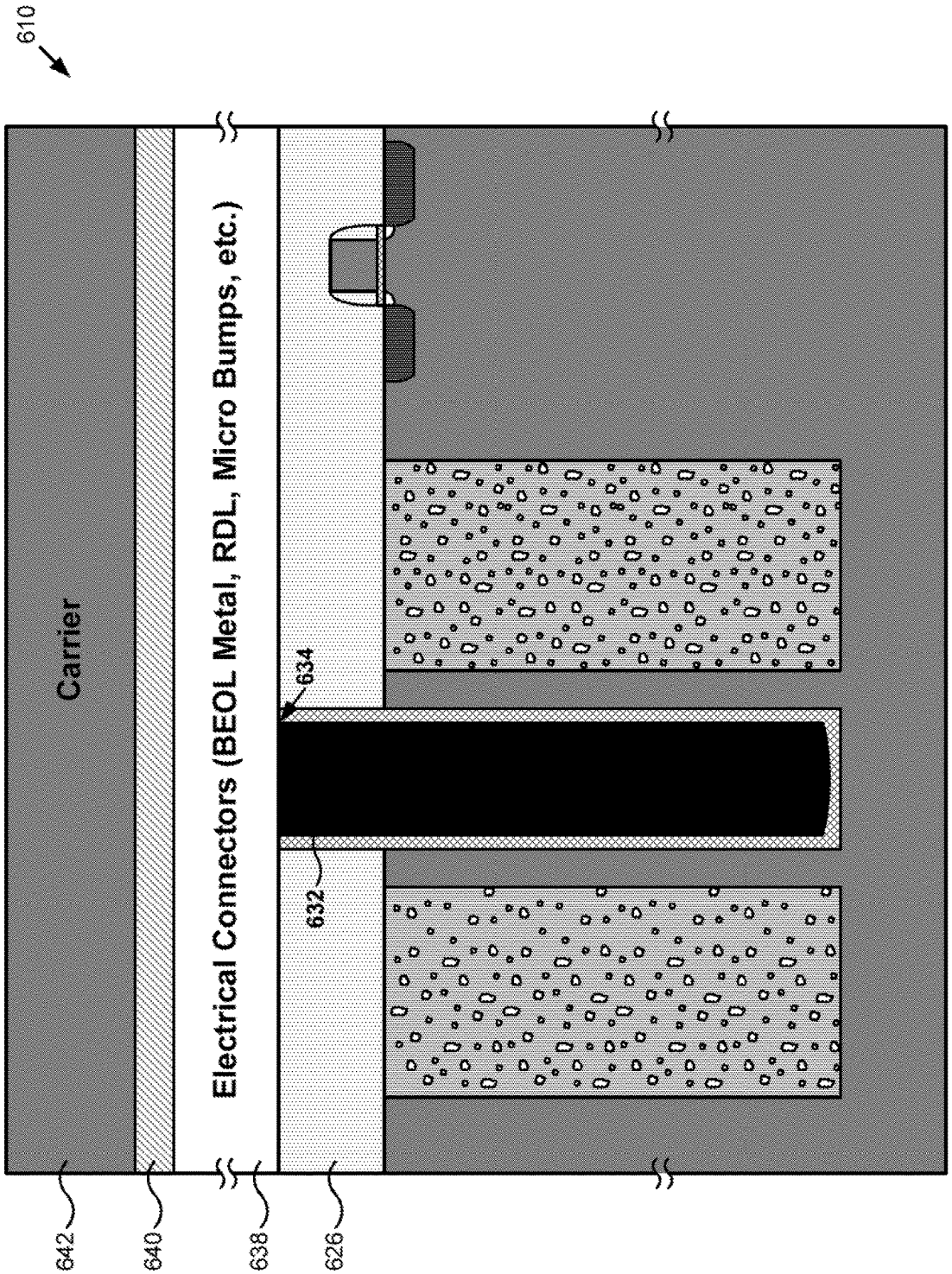
610
Carrier
Electrical Connectors (BEOL Metal, RDL, Micro Bumps, etc.)
634
632
642
640
638
626

FIG. 6F

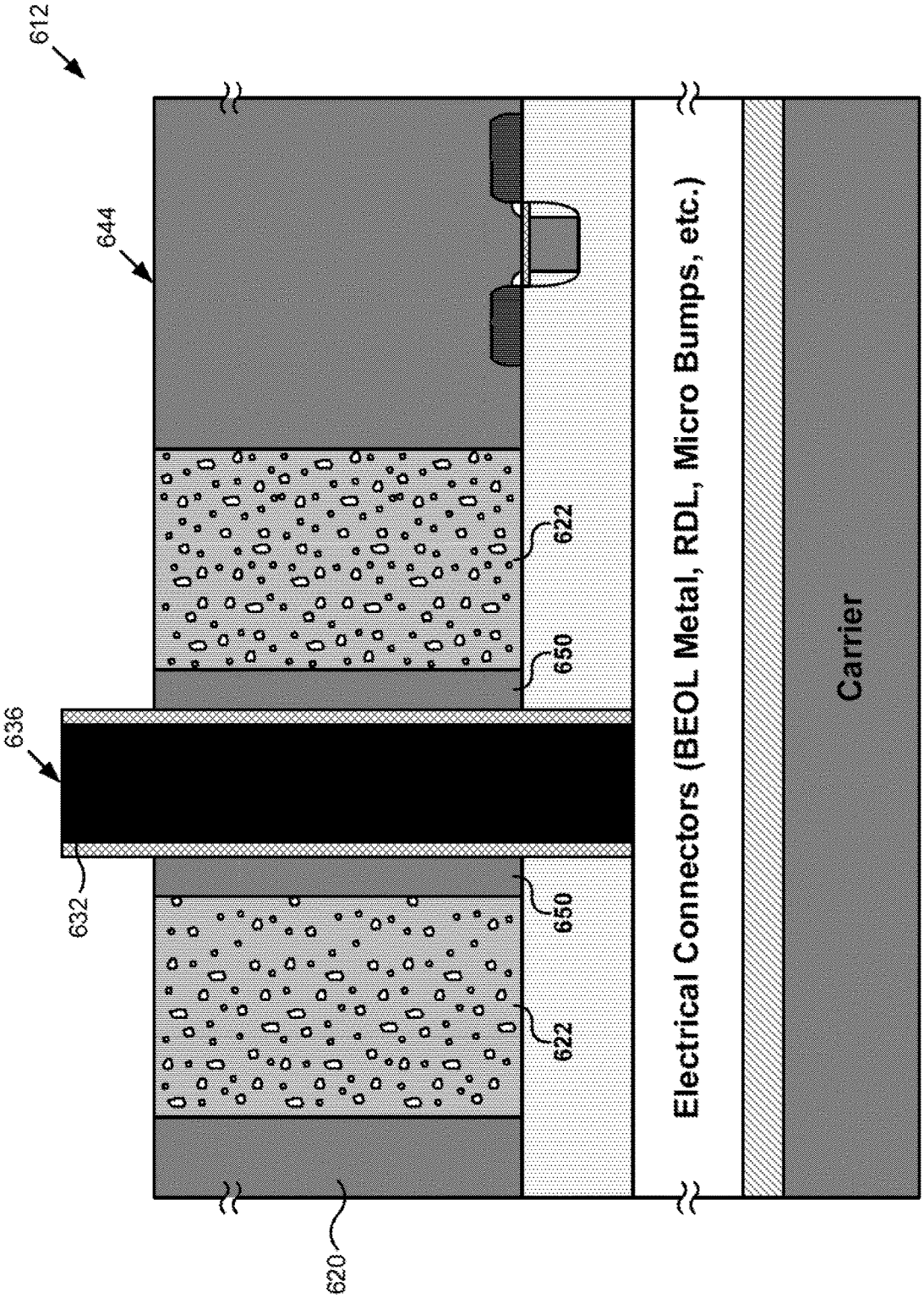
612
644
622
650
636
632
650
622
620
Electrical Connectors (BEOL Metal, RDL, Micro Bumps, etc.)
Carrier

FIG. 6G

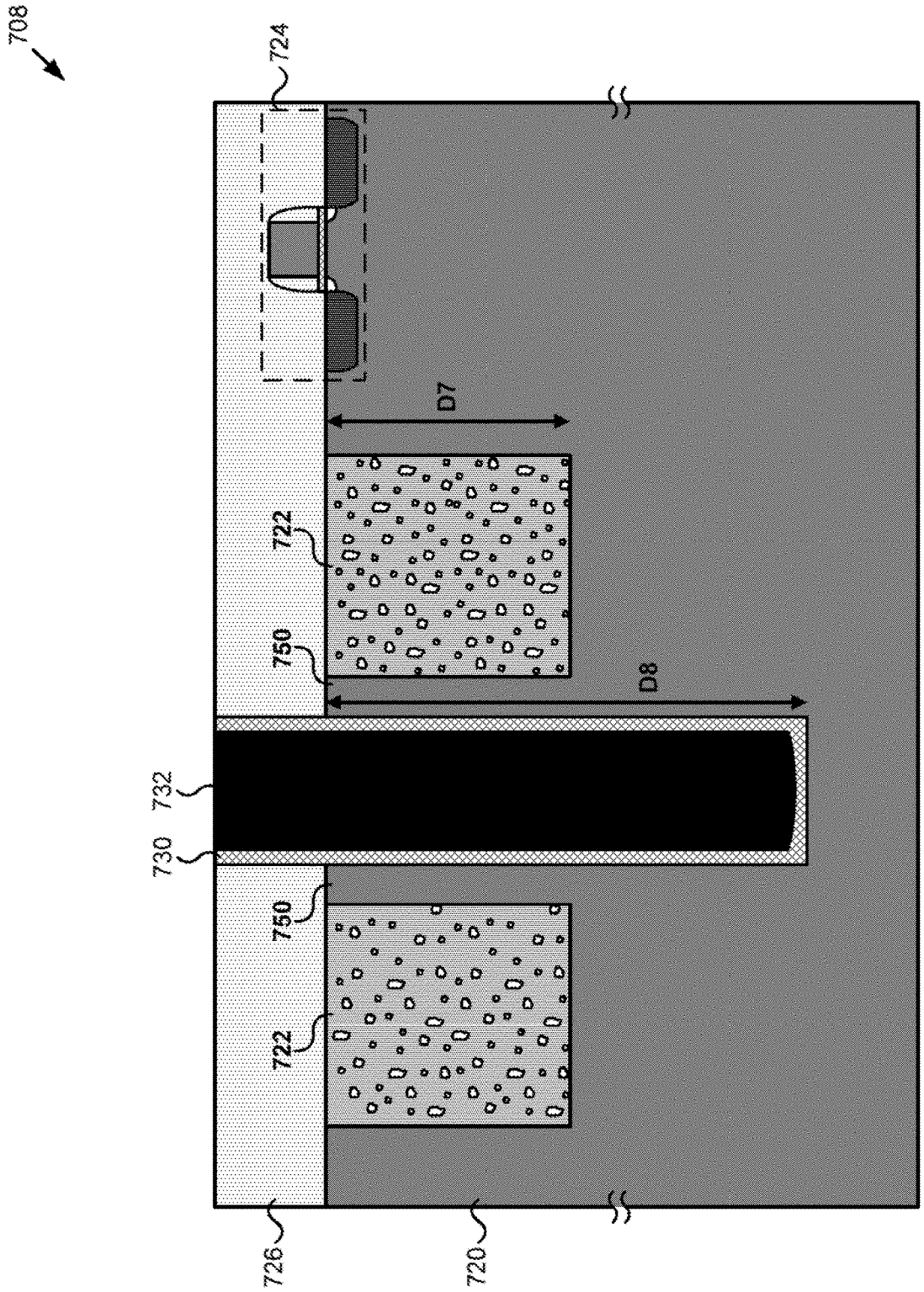

FIG. 7A

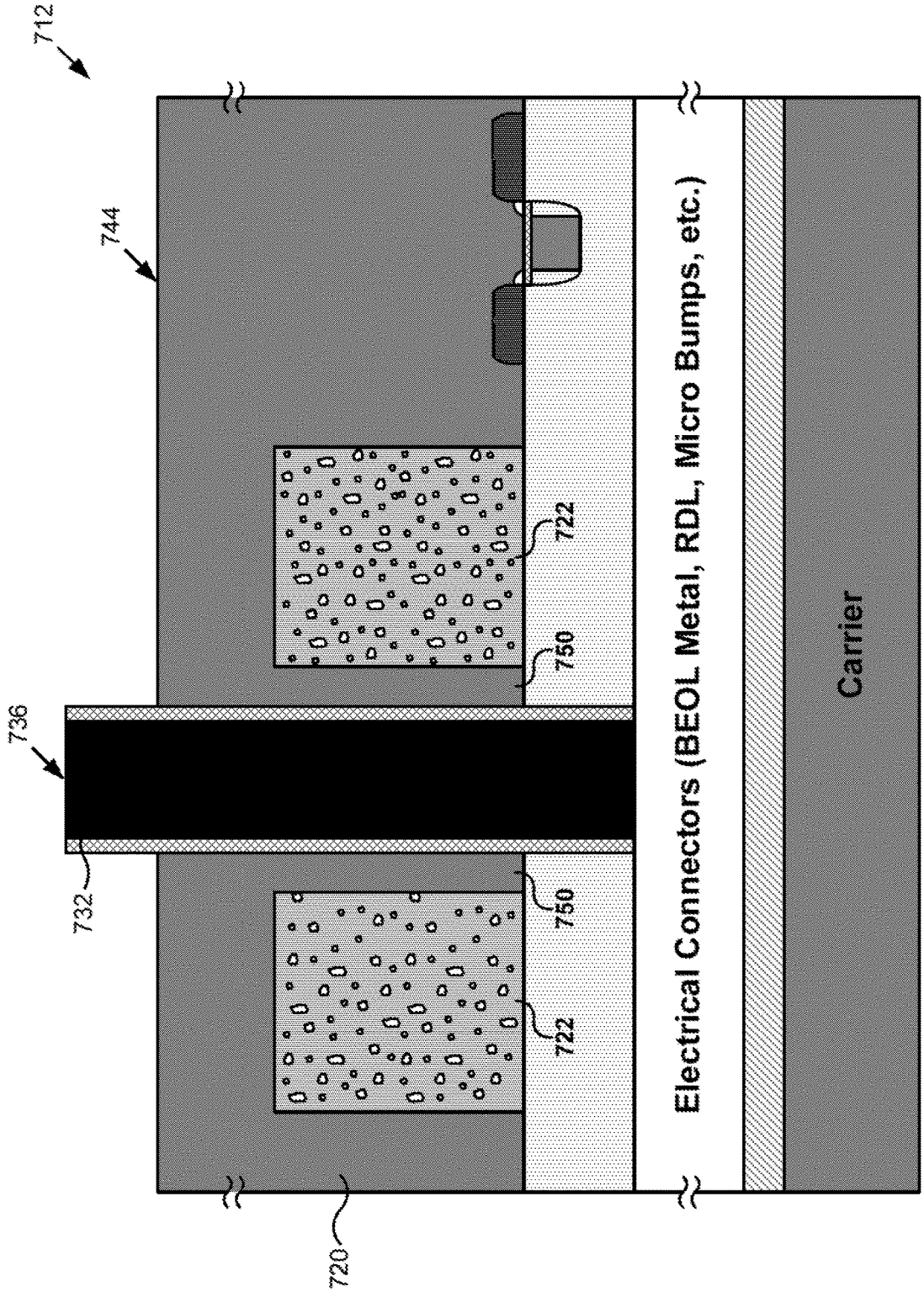
712
744
722
750
736
732
750
722
720
Electrical Connectors (BEOL Metal, RDL, Micro Bumps, etc.)
Carrier

FIG. 7B

SEMICONDUCTOR STRUCTURE HAVING THROUGH-SUBSTRATE VIA (TSV) IN POROUS SEMICONDUCTOR REGION

CLAIMS OF PRIORITY

The present application is a continuation-in-part of and claims the benefit of and priority to application Ser. No. 16/597,779 filed on Oct. 9, 2019 and titled "Semiconductor Structure Having Porous Semiconductor Layer for RF Devices,". The present application is also a continuation-in-part of and claims the benefit of and priority to application Ser. No. 16/598,803 filed on Oct. 10, 2019, titled "Semiconductor Structure Having Porous Semiconductor Segment for RF Devices and Bulk Semiconductor Region for Non-RF Devices,". The disclosures and contents of the above-identified applications are hereby incorporated fully by reference into the present application.

BACKGROUND

As known in the art, through-silicon (or through-substrate) vias (TSVs) generally pass through the entire bulk silicon substrate, and are utilized to, for example, create robust electrical connections. In "3D" integrated circuits where a semiconductor die connects to a printed circuit board or to another stacked semiconductor die, numerous TSVs might be used. However, TSVs have a high coefficient of thermal expansion (CTE) compared to bulk silicon; for example, approximately seventeen parts per million per degree Celsius (17 ppm/° C.) versus approximately three parts per million per degree Celsius (3 ppm/° C.), respectively. When the semiconductor structure is subjected to high temperatures, such as during operation of power amplifiers, during high ambient temperatures, or during BEOL processing utilized to form metallizations and other structures, this CTE mismatch increases the susceptibility of the semiconductor structure to thermal stresses. Also, significant shifts in ambient temperatures, i.e. temperatures getting too low or too high, may place the semiconductor structure under thermal stress. These thermal stresses could cause a variety of defects, such as cracking, metal diffusion, and/or current crowding.

Bulk silicon is also relatively rigid, and may have a Young's modulus of elasticity of approximately one hundred sixty gigapascals (160 GPa). The semiconductor structure with the TSVs may not withstand mechanical stresses when subjected to high forces, such as forces from chemical machine polishing (CMP) utilized to form metallizations and other structures, or forces from a semiconductor packaging process. These mechanical stresses could also cause cracking and other defects, just as thermal stresses would.

Thus, there is need in the art for robust semiconductor structures including TSVs that effectively withstand thermal and mechanical stresses.

SUMMARY

The present disclosure is directed to a semiconductor structure having a through-substrate via (TSV) in a porous semiconductor region, substantially as shown in and/or described in connection with at least one of the figures, and as set forth in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates a flowchart of an exemplary method for manufacturing a semiconductor structure according to one implementation of the present application.

FIG. **2**A illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with the flowchart of FIG. **1** according to one implementation of the present application.

FIG. **2**B illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with the flowchart of FIG. **1** according to one implementation of the present application.

FIG. **2**C illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with the flowchart of FIG. **1** according to one implementation of the present application.

FIG. **2**D illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with the flowchart of FIG. **1** according to one implementation of the present application.

FIG. **2**E illustrates a top cross-sectional view of a portion of a semiconductor structure corresponding to the semiconductor structure in FIG. **2**D according to one implementation of the present application.

FIG. **2**F illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with the flowchart of FIG. **1** according to one implementation of the present application.

FIG. **2**G illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with the flowchart of FIG. **1** according to one implementation of the present application.

FIG. **3** illustrates a flowchart of an exemplary method for manufacturing a semiconductor structure according to one implementation of the present application.

FIG. **4**A illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with the flowchart of FIG. **3** according to one implementation of the present application.

FIG. **4**B illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with the flowchart of FIG. **3** according to one implementation of the present application.

FIG. **4**C illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with the flowchart of FIG. **3** according to one implementation of the present application.

FIG. **4**D illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with the flowchart of FIG. **3** according to one implementation of the present application.

FIG. **4**E illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with the flowchart of FIG. **3** according to one implementation of the present application.

FIG. **4**F illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with the flowchart of FIG. **3** according to one implementation of the present application.

FIG. **5** illustrates a flowchart of an exemplary method for manufacturing a semiconductor structure according to one implementation of the present application.

FIG. **6**A illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with the flowchart of FIG. **5** according to one implementation of the present application.

FIG. **6**B illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with the flowchart of FIG. **5** according to one implementation of the present application.

FIG. **6**C illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with the flowchart of FIG. **5** according to one implementation of the present application.

FIG. **6**D illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with the flowchart of FIG. **5** according to one implementation of the present application.

FIG. **6**E illustrates a top cross-sectional view of a portion of a semiconductor structure corresponding to the semiconductor structure in FIG. **6**D according to one implementation of the present application.

FIG. **6**F illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with the flowchart of FIG. **5** according to one implementation of the present application.

FIG. **6**G illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with the flowchart of FIG. **5** according to one implementation of the present application.

FIG. **7**A illustrates a cross-sectional view of a portion of a semiconductor structure according to one implementation of the present application.

FIG. **7**B illustrates a cross-sectional view of a portion of a semiconductor structure corresponding to the semiconductor structure in FIG. **7**A according to one implementation of the present application.

DETAILED DESCRIPTION

The following description contains specific information pertaining to implementations in the present disclosure. The drawings in the present application and their accompanying detailed description are directed to merely exemplary implementations. Unless noted otherwise, like or corresponding elements among the figures may be indicated by like or corresponding reference numerals. Moreover, the drawings and illustrations in the present application are generally not to scale, and are not intended to correspond to actual relative dimensions.

FIG. **1** illustrates a flowchart of an exemplary method for manufacturing a semiconductor structure according to one implementation of the present application. Structures shown in FIGS. **2**A through **2**G illustrate the results of performing actions **102** through **112** shown in the flowchart of FIG. **1**. For example, FIG. **2**A shows a semiconductor structure after performing action **102** in FIG. **1**, FIG. **2**B shows a semiconductor structure after performing action **104** in FIG. **1**, and so forth.

Actions **102** through **112** shown in the flowchart of FIG. **1** are sufficient to describe one implementation of the present inventive concepts. Other implementations of the present inventive concepts may utilize actions different from those shown in the flowchart of FIG. **1**. Certain details and features have been left out of the flowchart of FIG. **1** that are apparent to a person of ordinary skill in the art. For example, an action may consist of one or more sub-actions or may involve specialized equipment or materials, as known in the art. Moreover, some actions, such as masking and cleaning actions, may be omitted so as not to distract from the illustrated actions.

FIG. **2**A illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with the flowchart of FIG. **1** according to one implementation of the present application. As shown in FIG. **2**A, semiconductor structure **202** is provided. Semiconductor structure **202** includes bulk silicon substrate **220**, porous silicon region **222**, semiconductor device **224**, and interlayer dielectric **226**.

In the present implementation, bulk silicon substrate **220** is a P− or P+ type single crystal silicon substrate. In various implementations, bulk silicon substrate **220** may be any other type of substrate. For example, bulk silicon substrate **220** can comprise germanium (Ge). In various implementations, bulk silicon substrate **220** can have a thickness of approximately seven hundred microns (700 μm) or greater or less.

Porous silicon region **222** is situated within bulk silicon substrate **220**. Porous silicon region **222** is a silicon region having voids, or pores, therein. Within porous silicon region **222**, the pores can have any orientation, branching, fill, or other morphological characteristic known in the art. Porous silicon region **222** can be formed by using a top-down technique, where portions of bulk silicon substrate **220** are removed to generate pores. In one implementation, a hard-mask is formed over bulk silicon substrate **220** to expose a segment thereof. Then, porous silicon region **222** is formed by electrochemical etching the exposed segment of bulk silicon substrate **220** using hydrofluoric acid (HF). Alternatively, porous silicon region **222** can be formed by stain etching, photoetching, or any other top-down technique known in the art.

In various implementations, porous silicon region **222** can also be formed by using a bottom-up technique, where deposition results in a silicon region having voids. For example, porous silicon region **222** can be formed by low-temperature high-density plasma (HDP) deposition, plasma hydrogenation of an amorphous layer, laser ablation, or any other bottom-up technique known in the art. Depth D**1** represents the depth of porous silicon region **222** measured from the top surface of bulk silicon substrate **220**. In various implementations, depth D**1** of porous silicon region **222** can be approximately two hundred fifty microns (250 μm). In various implementations, porous silicon region **222** can have any other depth. In various implementations, porous silicon region **222** may be a semiconductor material other than silicon.

Semiconductor structure **202** includes semiconductor device **224**. In the present implementation, semiconductor device **224** is a transistor. In various implementations, semiconductor device **224** can be a power amplifier, a filter, a mixer, a diode, or a micro-electromechanical systems (MEMS) device. In various implementations, semiconductor device **224** can be an active circuit comprising multiple active devices, or comprising passive devices in combination with at least one active device. As described below, semiconductor device **224** can be a source of stress in semiconductor structure **202**.

Interlayer dielectric **226** is situated over bulk silicon substrate **220**, porous silicon region **222**, and semiconductor device **224**. Interlayer dielectric **226** can comprise, for example, silicon dioxide (SiO_2), phosphosilicate glass (PSG), or another dielectric. Interlayer dielectric **226** and semiconductor device **224** can correspond to a front-end-of-line (FEOL) in an integrated circuit (IC) process. Electrical connectors (not shown in FIG. **2**A) for connecting to semiconductor device **224** can be situated in interlayer dielectric **226**.

FIG. **2**B illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **104** in the flowchart of FIG. **1** according to one

implementation of the present application. As shown in FIG. **2**B, in semiconductor structure **204**, trench **228** is formed in porous silicon region **222**.

Trench **228** extends through interlayer dielectric **226** and into porous silicon region **222**. In one implementation, trench **228** is formed using a fluorine-based anisotropic etch. In another implementation, trench **228** is formed using the Bosch etch process known in the art. Notably, because the etch rate of porous silicon is generally faster than the etch rate of bulk silicon, trench **228** formed in porous silicon region **222** can be formed faster than a trench formed in bulk silicon.

Depth D**2** represents the depth of trench **228** measured fro the top surface of bulk silicon substrate **220** that may or may not be as great as depth D**1** of porous silicon region **222**. In the present implementation, depth D**1** of porous silicon region **222** in bulk silicon substrate **220** is substantially equal to depth D**2** of trench **228**. Alternatively, depth D**1** of porous silicon region **222** can be greater than depth D**2** of trench **228**. The timing of an etching action utilized to form trench **228** can be shortened to ensure that depth D**1** of porous silicon region **222** is greater than depth D**2** of trench **228**. In various implementations, depth D**2** of trench **228** can range from approximately fifty microns to approximately two hundred fifty microns (50 μm-250 μm), while a width of trench **228** can range from approximately three microns to approximately fifty microns (3 μm-50 μm). In various implementations, the aperture of trench **228** (not shown in FIG. **2**B) can have a circular shape, a rectangular shape, or any other shape.

In FIG. **2**B, trench **228** is formed after semiconductor device **224** and interlayer dielectric **226**, but before any interconnect metal levels of a back-end-of-line multi-level metallization (BEOL MLM). In one implementation, trench **228** can be formed before semiconductor device **224** and interlayer dielectric **226**. In this implementation, trench **228** can extend through porous silicon region **222**, without extending through interlayer dielectric **226**. In another implementation, trench **228** can be formed as part of a BEOL MLM (not shown in FIG. **2**B) situated over interlayer dielectric **226**. For example, trench **228** can extend from a third interconnect metal level (i.e., M3) into porous silicon region **222**. In yet another implementation, trench **228** can be formed after a BEOL MLM (not shown in FIG. **2**B).

FIG. **2**C illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **106** in the flowchart of FIG. **1** according to one implementation of the present application. As shown in FIG. **2**C, in semiconductor structure **206**, dielectric liner **230** is formed in trench **228**.

Dielectric liner **230** lines trench **228**. As shown in FIG. **2**C, dielectric liner **230** is formed over porous silicon region **222** and interlayer dielectric **226** along sidewalls of trench **228**, and over bulk silicon substrate **220** at a bottom of trench **228**. Dielectric liner **230** can be formed, for example, by plasma enhanced chemical vapor deposition (PECVD) or high density plasma CVD (HDP-CVD). Dielectric liner **230** can comprise, for example, silicon oxide (Si_XO_Y). In various implementations, dielectric liner **230** is a low-k dielectric. In one implementation, the thickness of dielectric liner **230** can range from approximately two hundred angstroms to approximately five hundred angstroms (200 Å-500 Å).

Where depth D**1** (shown in FIG. **2**B) of porous silicon region **222** is greater than depth D**2** (shown in FIG. **2**B) of trench **228**, dielectric liner **230** can be formed over porous silicon region **222** at a bottom of trench **228**, rather than over bulk silicon substrate **220**. As shown in FIG. **2**C, dielectric liner **230** is planarized with interlayer dielectric **226**. In other implementations, segments of dielectric liner **230** can remain over interlayer dielectric **226**. Dielectric liner **230** is considered optional in that semiconductor structures according to the present application can be formed without dielectric liner **230**.

FIG. **2**D illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **108** in the flowchart of FIG. **1** according to one implementation of the present application. As shown in FIG. **2**D, in semiconductor structure **208**, through-substrate via (TSV) **232** is formed in trench **228** over dielectric liner **230**.

TSV **232** can be formed, for example, by a damascene process. TSV **232** can comprise, for example, copper (Cu), aluminum (Al), or titanium (Ti). As shown in FIG. **2**D, TSV **232** is planarized with interlayer dielectric **226**. In other implementations, segments of a metal utilized to form TSV **232** can remain over interlayer dielectric **226** and/or dielectric liner **230**. In various implementations, a barrier layer (not shown in FIG. **2**D) can be formed prior to TSV **232**.

In FIG. **2**D, porous silicon region **222** has a coefficient of thermal expansion (CTE) that more closely matches a CTE of TSV **232**, compared to a CTE of bulk silicon substrate **220**. For example, bulk silicon substrate **220** may have a CTE of approximately three parts per million per degree Celsius (3 ppm/° C.), whereas TSV **232** comprising copper may have a CTE of approximately seventeen parts per million per degree Celsius (17 ppm/° C.). This CTE mismatch increases the susceptibility of semiconductor structure **208** and/or TSV **232** to thermal stresses. However, CTE of porous silicon is significantly greater than bulk silicon. As such, if porous silicon region **222** were not used, semiconductor structure **208** and/or TSV **232** may not withstand thermal stresses when subjected to high temperatures, such as during operation of semiconductor device **224**, during high ambient temperatures, or during BEOL processing utilized to form metallizations and other structures over semiconductor structure **208**. Also, significant shifts in ambient temperatures, temperatures getting too low or too high, may place semiconductor structure **208** under thermal stress. These thermal stresses could cause a variety of defects, such as cracking of TSV **232**, dielectric liner **230**, and/or bulk silicon substrate **220**, or metal diffusion of TSV **232** into bulk silicon substrate **220**. In contrast, porous silicon region **222** has a CTE significantly greater than the CTE of bulk silicon substrate **220**. The CTE of porous silicon region **222** more closely matches the CTE of TSV **232**. Accordingly, because TSV **232** is situated within porous silicon region **222**, porous silicon region **222** causes semiconductor structure **208** and/or TSV **232** to withstand thermal stresses.

Porous silicon region **222** is also more deformable than bulk silicon substrate **220**. For example, bulk silicon substrate **220** may be relatively rigid and have a Young's modulus of elasticity of approximately one hundred sixty gigapascals (160 GPa), whereas porous silicon region **222** may be relatively deformable and have a Young's modulus of elasticity of approximately sixty gigapascals (60 GPa). For porous silicon region **222**, deformability generally increases as porosity increases. If porous silicon region **222** were not used, semiconductor structure **208** and/or TSV **232** may not withstand mechanical stresses when subjected to high forces, such as forces from chemical machine polishing (CMP) utilized to form metallizations and other structures, or forces from a semiconductor packaging process. These mechanical stresses could cause cracking of TSV **232**, dielectric liner **230**, and/or bulk silicon substrate **220**. In

contrast, porous silicon region **222** is more deformable than bulk silicon substrate **220**. Accordingly, because TSV **232** is situated within porous silicon region **222**, porous silicon region **222** causes semiconductor structure **208** and/or TSV **232** to withstand mechanical stresses.

Further, porous silicon region **222** reduces signal leakage and parasitic capacitive coupling between TSV **232** and bulk silicon substrate **220**. Pores in porous silicon region **222** decrease its effective dielectric constant and increase its resistivity. In semiconductor structure **208** in FIG. **2**D, porous silicon region **222** has a dielectric constant significantly less than the dielectric constant of bulk silicon substrate **220**. For example, bulk silicon substrate **220** may have a dielectric constant of approximately 11.7, and porous silicon region **222** may have a dielectric constant significantly less than 11.7. In particular, porous silicon region **222** can have a dielectric constant from approximately 2.0 to approximately 4.0. As a result, in various implementations, dielectric liner **230** can be kept thin or not used altogether.

FIG. **2**E illustrates a top cross-sectional view of a portion of a semiconductor structure corresponding to the semiconductor structure in FIG. **2**D according to one implementation of the present application. FIG. **2**E represents a cross-sectional view along line "**2**E-**2**E" in FIG. **2**D.

As shown in FIG. **2**E, semiconductor structure **208** includes bulk silicon substrate **220**, porous silicon region **222**, dielectric liner **230**, and TSV **232**. Porous silicon region **222** is situated within bulk silicon substrate **220**, and TSV **232** is situated within porous silicon region **222**. As described above, because porous silicon region **222** provides better CTE matching with TSV **232** compared to bulk silicon substrate **220**, and because porous silicon region **222** is more deformable compared to bulk silicon substrate **220**, porous silicon region **222** causes semiconductor structure **208** and/or TSV **232** to withstand thermal and mechanical stresses. In the present implementation, porous silicon region **222**, dielectric liner **230**, and TSV **232** have a substantially circular shape. In various implementations, porous silicon region **222**, dielectric liner **230**, and TSV **232** can have a rectangular shape, or any other shape.

FIG. **2**F illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **110** in the flowchart of FIG. **1** according to one implementation of the present application. As shown in FIG. **2**F, in semiconductor structure **210**, electrical connection layer **238** is formed over TSV **232** and over interlayer dielectric **226**. Electrical connection layer **238** contains at least one electrical connector situated over front end **234** of TSV **232**.

Electrical connection layer **238** can comprise generally any BEOL MLM suitable for semiconductor devices. Electrical connection layer **238** can also comprise a redistribution layer (RDL), micro bumps, and/or contact pads. Electrical connection layer **238** can also comprise a plurality of devices, such as integrated passive devices (IPDs; not shown in FIG. **2**F). Electrical connection layer **238** can be much larger than shown in FIG. **2**F.

Any electrical connector in electrical connection layer **238** can be situated over front end **234** of TSV **232**. For example, in one implementation, TSV **232** can be formed as part of a BEOL MLM, and a third interconnect metal (i.e., M3) can be situated over front end **234** of TSV **232**. As another example, in one implementation, TSV **232** can be formed before interlayer dielectric **226**, and another via or an IPD can be situated over front end **234** of TSV **232**. As yet another example, in one implementation, TSV **232** can be formed after a BEOL MLM, and a redistribution metal or a micro bump can be situated over front end **234** of TSV **232**. In various implementations, the electrical connector situated over front end **234** of TSV **232** can comprise, for example, Cu, Al or Ti.

As described above, semiconductor structure **210** and/or TSV **232** can experience thermal and mechanical stresses. If porous silicon region **222** were not used, these stresses could cause defects in an electrical connector situated over front end **234** of TSV **232** in electrical connection layer **238**. For example, thermal expansion of TSV **232** could create a shear force in a micro bump situated over front end **234** of TSV **232** and cause the micro bump to crack, which could also lead to current crowding. Although larger electrical connectors can be utilized to help withstand stress, using larger electrical connectors also prohibits downsizing and reduces interconnect density. Moreover, in "3D" integrated circuits where semiconductor structure **210** connects to a printed circuit board or to another stacked semiconductor structure, numerous TSVs might be used, exacerbating these effects. In semiconductor structure **210** in FIG. **2**F, because TSV **232** is situated within porous silicon region **222**, porous silicon region **222** causes electrical connectors in electrical connection layer **238** to withstand thermal and mechanical stresses, without reducing interconnect density.

As shown in FIG. **2**F, electrical connection layer **238** is temporarily bonded with carrier wafer **242** by bonding layer **240**. In various implementations, carrier wafer **242** can be glass, quartz, or silicon. In various implementations, bonding layer **240** is a curable polymeric adhesive or a thermoplastic adhesive utilized to bond electrical connection layer **238** with carrier wafer **242**. Alternatively, electrical connection layer **238** can be bonded with carrier wafer **242** using any other bonding technique known in the art. Carrier wafer **242** allows semiconductor structure **210** to be flipped such that carrier wafer **242** is on bottom and bulk silicon substrate **220** is on top, to allow subsequent fabricating actions to be performed on bulk silicon substrate **220**.

FIG. **2**G illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **112** in the flowchart of FIG. **1** according to one implementation of the present application. As shown in FIG. **2**G, in semiconductor structure **212**, porous silicon region **222** and bulk silicon substrate **220** are both etched, and back end **236** of TSV **232** is revealed from backside **244** of bulk silicon substrate **220**.

Bulk silicon substrate **220** can be thinned using a wafer grind and/or CMP prior to revealing back end **236** of TSV **232**. Then, a wet etch, for example, using potassium hydroxide (KOH) or tetramethylammonium hydroxide (TMAH), or a dry plasma etch, for example, using sulfur hexafluoride (SF6), can be utilized to etch porous silicon region **222** and bulk silicon substrate **220** without etching dielectric liner **230** and TSV **232**. Then, a portion of dielectric liner **230** over back end **236** of TSV **232** can be removed by CMP to reveal back end **236** of TSV **232**. Back end **236** of TSV **232** can also be polished when dielectric liner **230** is polished. Then, electrical connectors and/or other packaging (not shown in FIG. **2**G) can be formed over back end **236** of TSV **232**.

In an alternative implementation, after etching porous silicon region **222** and bulk silicon substrate **220**, a dielectric layer (not shown in FIG. **2**G) can be formed over porous silicon region **222**, bulk silicon substrate **220**, and dielectric liner **230**. Then, CMP can be utilized to remove dielectric liner **230** from back end **236** of TSV **232**, and to concurrently planarize the dielectric layer (not shown in FIG. **2**G) with back end **236** of TSV **232**. In another implementation,

after etching porous silicon region **222** and bulk silicon substrate **220**, a portion of dielectric liner **230** over back end **236** of TSV **232** can be removed by a fluorine-based wet etch. In yet another implementation, back end **236** of TSV **232** can be exposed by using a single CMP action to remove dielectric liner **230** from back end **236** of TSV **232**, and to concurrently remove portions of porous silicon region **222**, bulk silicon substrate **220**, and TSV **232**.

Notably, porous silicon region **222** and bulk silicon substrate **220** are both etched to reveal back end **236** of TSV **232**. As shown in FIG. **2**F, prior to revealing back end **236** of TSV **232**, the depth of porous silicon region **222** in bulk silicon substrate **220** was greater than or equal to the depth of TSV **232** in bulk silicon substrate **220**. As a result, after revealing back end **236** of TSV **232** as shown in FIG. **2**G, porous silicon region **222** extends substantially to backside **244** of bulk silicon substrate **220**. Accordingly, porous silicon region **222** greatly improves the ability of semiconductor structure **212** and/or TSV **232** to withstand thermal and mechanical stresses.

FIG. **3** illustrates a flowchart of an exemplary method for manufacturing a semiconductor structure according to one implementation of the present application. Structures shown in FIGS. **4**A through **4**F illustrate the results of performing actions **302** through **312** shown in the flowchart of FIG. **3**. For example, FIG. **4**A shows a semiconductor structure after performing action **302** in FIG. **3**, FIG. **4**B shows a semiconductor structure after performing action **304** in FIG. **3**, and so forth.

Actions **302** through **312** shown in the flowchart of FIG. **3** are sufficient to describe one implementation of the present inventive concepts. Other implementations of the present inventive concepts may utilize actions different from those shown in the flowchart of FIG. **3**. Certain details and features have been left out of the flowchart of FIG. **3** that are apparent to a person of ordinary skill in the art. For example, an action may consist of one or more sub-actions or may involve specialized equipment or materials, as known in the art. Moreover, some actions, such as masking and cleaning actions, may be omitted so as not to distract from the illustrated actions.

Unlike in action **104** in the flowchart of FIG. **1**, wherein a depth of the porous semiconductor region is greater than or equal to a depth of the trench, in action **304** in the flowchart of FIG. **3**, a depth of the porous semiconductor region is less than a depth of the trench. Also, unlike in action **112** in the flowchart of FIG. **1**, wherein the porous semiconductor region is etched to reveal a back end of the TSV, in action **312** in the flowchart of FIG. **3**, only the semiconductor substrate is etched to reveal a back end of the TSV. Except for differences described above, the flowchart of FIG. **3** generally corresponds to the flowchart of FIG. **1**, and may have any implementations and advantages described above.

FIG. **4**A illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **302** in the flowchart of FIG. **3** according to one implementation of the present application. As shown in FIG. **4**A, semiconductor structure **402** is provided. Semiconductor structure **402** includes bulk silicon substrate **420**, porous silicon region **422**, semiconductor device **424**, and interlayer dielectric **426**.

Depth D**3** represents the depth of porous silicon region **422** measured from the top surface of bulk silicon substrate **420**. In various implementations, depth D**3** of porous silicon region **422** can be approximately fifty microns (50 μm). In various implementations, porous silicon region **422** can have any other depth. Notably, depth D**3** of porous silicon region **422** in FIG. **4**A is less than depth D**1** of porous silicon region **222** in FIG. **2**A. Except for differences described above, semiconductor structure **402** in FIG. **4**A generally corresponds to semiconductor structure **202** in FIG. **2**A, and may have any implementations and advantages described above.

FIG. **4**B illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **304** in the flowchart of FIG. **3** according to one implementation of the present application. As shown in FIG. **4**B, in semiconductor structure **404**, trench **428** is formed in porous silicon region **422**. Trench **428** extends through interlayer dielectric **426**, through porous silicon region **422**, and into bulk silicon substrate **420**.

Depth D**4** represents the depth of trench **428** measured fro the top surface of bulk silicon substrate **420**. In the present implementation, depth D**3** of porous silicon region **422** is substantially less than depth D**4** of trench **428**. The timing of an etching action utilized to form trench **428** can be lengthened to ensure that depth D**3** of porous silicon region **422** is less than depth D**4** of trench **428**. In various implementations, depth D**4** of trench **428** can range from approximately fifty microns to approximately two hundred fifty microns (50 μm-250 μm). In one implementation, depth D**3** of porous silicon region **422** is approximately ten microns (10 μm) less than depth D**4** of trench **428** to ensure that porous silicon region **422** is not damaged in a subsequent reveal action. For example, depth D**3** of porous silicon region **422** can be approximately ninety microns (90 μm), while depth D**4** of trench **428** can be approximately one hundred microns (100 μm). Except for differences described above, semiconductor structure **404** in FIG. **4**B generally corresponds to semiconductor structure **204** in FIG. **2**B, and may have any implementations and advantages described above.

FIG. **4**C illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **306** in the flowchart of FIG. **3** according to one implementation of the present application. As shown in FIG. **4**C, in semiconductor structure **406**, dielectric liner **430** is formed in trench **428**.

Unlike in FIG. **2**C, wherein dielectric liner **230** is formed over porous silicon region **222** and interlayer dielectric **226** along sidewalls of trench **228**, dielectric liner **430** in FIG. **4**C is additionally formed over bulk silicon substrate **220** on sidewalls of trench **428**. Except for differences described above, semiconductor structure **406** in FIG. **4**C generally corresponds to semiconductor structure **206** in FIG. **2**C, and may have any implementations and advantages described above.

FIG. **4**D illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **308** in the flowchart of FIG. **3** according to one implementation of the present application. As shown in FIG. **4**D, in semiconductor structure **408**, TSV **432** is formed in trench **428** over dielectric liner **430**.

Unlike in FIG. **2**D, wherein a depth of porous silicon region **222** is greater than or equal to a depth of TSV **232**, in FIG. **4**C, a depth of porous silicon region **422** is less than a depth of TSV **432**. Accordingly, TSV **432** in FIG. **4**D is additionally situated within bulk silicon substrate **420**. Except for differences described above, semiconductor structure **408** in FIG. **4**D generally corresponds to semiconductor structure **208** in FIG. **2**D, and may have any implementations and advantages described above.

FIG. **4**E illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **310** the flowchart of FIG. **3** according to one imple-

mentation of the present application. As shown in FIG. **4**E, in semiconductor structure **410**, electrical connection layer **438** is formed over TSV **432** and over interlayer dielectric **426**. Electrical connection layer **438** contains at least one electrical connector situated over front end **434** of TSV **432**. Also, electrical connection layer **438** is temporarily bonded with carrier wafer **442** by bonding layer **440**. Semiconductor structure **410** in FIG. **4**E generally corresponds to semiconductor structure **210** in FIG. **2**F, and may have any implementations and advantages described above.

FIG. **4**F illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **312** the flowchart of FIG. **3** according to one implementation of the present application. As shown in FIG. **4**F, in semiconductor structure **412**, bulk silicon substrate **420** is etched, and back end **436** of TSV **432** is revealed from backside **444** of bulk silicon substrate **420**.

Unlike in FIG. **2**G, wherein porous silicon region **222** and bulk silicon substrate **220** are both etched, in FIG. **4**F, only bulk silicon substrate **420** is etched. When revealing back end **236** of TSV **232** as shown in FIG. **2**G, pores of porous silicon region **222** can absorb solutions utilized in the etching action. These solutions cannot be easily removed from porous silicon region **222**, and can damage porous silicon region **222** and/or reduce the ability of porous silicon region **222** to withstand thermal and mechanical stresses.

As shown in FIG. **4**E, prior to revealing back end **436** of TSV **432**, the depth of porous silicon region **422** in bulk silicon substrate **420** was less than the depth of TSV **432** in bulk silicon substrate **420**. In one implementation, the depth of porous silicon region **422** relative to TSV **432** is determined based on a process parameter of the reveal action. For example, where the reveal action is only accurate to five microns (5 μm), the depth of porous silicon region **422** can be approximately ten microns (10 μm) less than the depth of TSV **432** to ensure that porous silicon region **422** is not damaged in the reveal action. For example, the depth of porous silicon region **422** can be approximately ninety microns (90 μm), while the depth of TSV **432** can be approximately one hundred microns (100 μm).

As a result, after revealing back end **436** of TSV **432** as shown in FIG. **4**F, porous silicon region **422** remains substantially unetched. A portion of bulk silicon substrate **420** intervenes between porous silicon region **422** and backside **444**, and is situated against the sides of TSV **432** (or against the sides of dielectric liner **430** in case dielectric liner **430** is used). Porous silicon region **422** still improves the ability of semiconductor structure **412** and/or TSV **432** to withstand thermal and mechanical stresses. Moreover, porous silicon region **422** does not absorb any etching solutions and provides increased reliability. It is noted that porous silicon region **422** and TSV **432** in FIGS. **4**E and **4**F are not drawn to scale, and may be exaggerated for purposes of illustration. Except for differences described above, semiconductor structure **412** in FIG. **4**F generally corresponds to semiconductor structure **212** in FIG. **2**G, and may have any implementations and advantages described above.

FIG. **5** illustrates a flowchart of an exemplary method for manufacturing a semiconductor structure according to one implementation of the present application. Structures shown in FIGS. **6**A through **6**G illustrate the results of performing actions **502** through **512** shown in the flowchart of FIG. **5**. For example, FIG. **6**A shows a semiconductor structure after performing action **502** in FIG. **5**, FIG. **6**B shows a semiconductor structure after performing action **504** in FIG. **5**, and so forth.

Actions **502** through **512** shown in the flowchart of FIG. **5** are sufficient to describe one implementation of the present inventive concepts. Other implementations of the present inventive concepts may utilize actions different from those shown in the flowchart of FIG. **5**. Certain details and features have been left out of the flowchart of FIG. **5** that are apparent to a person of ordinary skill in the art. For example, an action may consist of one or more sub-actions or may involve specialized equipment or materials, as known in the art. Moreover, some actions, such as masking and cleaning actions, may be omitted so as not to distract from the illustrated actions.

Unlike in action **102** in the flowchart of FIG. **1**, wherein a semiconductor structure includes a porous semiconductor region within a semiconductor substrate, in action **502** in the flowchart of FIG. **5**, a semiconductor structure additionally includes a semiconductor buffer ring within the porous semiconductor region. Also, unlike in action **104** in the flowchart of FIG. **1**, wherein a trench is formed in the porous semiconductor region, in action **504** in the flowchart of FIG. **5**, a trench is formed in the semiconductor buffer ring. Except for differences described above, the flowchart of FIG. **5** generally corresponds to the flowchart of FIG. **1**, and may have any implementations and advantages described above.

FIG. **6**A illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **502** in the flowchart of FIG. **5** according to one implementation of the present application. As shown in FIG. **6**A, semiconductor structure **602** is provided. Semiconductor structure **602** includes bulk silicon substrate **620**, porous silicon regions **622**, semiconductor device **624**, interlayer dielectric **626**, and silicon buffer ring **650**.

Silicon buffer ring **650** is situated within porous silicon regions **622**. In one implementation, a hardmask is formed over bulk silicon substrate **620** to expose segments thereof. Then, porous silicon regions **622** is formed by electrochemical etching the exposed segments of bulk silicon substrate **620** using hydrofluoric acid (HF). Unlike the hardmask utilized to form porous silicon region **222** in FIG. **2**A, the hardmask utilized to form porous silicon regions **622** in FIG. **6**A can cover an additional segment of bulk silicon substrate **620**, such that silicon buffer ring **650** remains after porous silicon regions **622** are formed. In various implementations, silicon buffer ring **650** may be a semiconductor material other than silicon.

Depth D**5** represents the depth of porous silicon region **622** measured from the top surface of bulk silicon substrate **620**. In various implementations, depth D**5** of porous silicon regions **622** can be approximately two hundred fifty microns (250 μm). In various implementations, porous silicon regions **622** can have any other depth. Notably, although porous silicon regions **622** are illustrated as distinct regions in the cross-sectional view in FIG. **6**A, in various implementations, porous silicon regions **622** can be integrally formed as a single porous silicon region, connected in a plane not illustrated in FIG. **6**A. Except for differences described above, semiconductor structure **602** in FIG. **6**A generally corresponds to semiconductor structure **202** in FIG. **2**A, and may have any implementations and advantages described above.

FIG. **6**B illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **504** in the flowchart of FIG. **5** according to one implementation of the present application. As shown in FIG. **6**B, in semiconductor structure **604**, trench **628** is formed in silicon buffer ring **650**.

Trench **628** extends through interlayer dielectric **626** and into silicon buffer ring **650**. In various implementations, a width of silicon buffer ring **650** between trench **628** and an adjacent one of porous silicon regions **622** can range from approximately two microns to approximately ten microns (2 μm-10 μm). Depth D**6** represents the depth of trench **628** measured from the top surface of bulk silicon substrate **620** that may or may not be as great as depth D**5** of porous silicon region **622**. In the present implementation, depth D**5** of porous silicon regions **622** is substantially equal to depth D**6** of trench **628**. Alternatively, depth D**5** of porous silicon regions **622** can be greater than depth D**6** of trench **628**. The timing of an etching action utilized to form trench **628** can be shortened to ensure that depth D**5** of porous silicon regions **622** is greater than depth D**6** of trench **628**. In various implementations, depth D**6** of trench **628** can range from approximately fifty microns to approximately two hundred fifty microns (50 μm-250 μm). Except for differences described above, semiconductor structure **604** in FIG. **6**B generally corresponds to semiconductor structure **204** in FIG. **2**B, and may have any implementations and advantages described above.

FIG. **6**C illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **506** in the flowchart of FIG. **5** according to one implementation of the present application. As shown in FIG. **6**C, in semiconductor structure **606**, dielectric liner **630** is formed in trench **628**.

Unlike in FIG. **2**C, wherein dielectric liner **230** is formed over porous silicon region **222** along sidewalls of trench **228**, dielectric liner **630** in FIG. **6**C is formed over silicon buffer ring **650** on sidewalls of trench **628**. Because silicon buffer ring **650** is a homogeneous single crystal surface, dielectric liner **630** can be deposited substantially conformably in trench **628**. If silicon buffer ring **650** were not used, and a dielectric liner were instead deposited in a trench having porous sidewalls as shown in FIG. **2**C, nonconformities can occur in the deposited dielectric liner, especially where the sidewalls are highly porous. Except for differences described above, semiconductor structure **606** in FIG. **6**C generally corresponds to semiconductor structure **206** in FIG. **2**C, and may have any implementations and advantages described above.

FIG. **6**D illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **508** in the flowchart of FIG. **5** according to one implementation of the present application. As shown in FIG. **6**D, in semiconductor structure **608**, TSV **632** is formed in trench **628** over dielectric liner **630**.

As described above, porous silicon regions **622** provide better effective CTE matching with TSV **632** compared to bulk silicon substrate **620**, and porous silicon regions **622** are more deformable compared to bulk silicon substrate **620**. Where a width of silicon buffer ring **650** between TSV **632** and one of porous silicon regions **622** is kept small, porous silicon regions **622** and silicon buffer ring **650** cause semiconductor structure **608** and/or TSV **632** to withstand thermal and mechanical stresses. At the same time, because TSV **632** in FIG. **6**D (or dielectric liner **630** in case dielectric liner **630** is used) interfaces with silicon buffer ring **650**, rather than interfacing with a porous silicon region as shown in FIG. **2**D, metal of TSV **632** is less likely to diffuse.

Further, because silicon buffer ring **650** is a homogeneous single crystal surface, TSV **632** can be formed substantially uniformly in trench **628**. If silicon buffer ring **650** were not used, and a TSV were instead formed in a trench having porous sidewalls as shown in FIG. **2**D, nonconformities can occur in the TSV, especially where the sidewalls are highly porous. Except for differences described above, semiconductor structure **608** in FIG. **6**D generally corresponds to semiconductor structure **208** in FIG. **2**D, and may have any implementations and advantages described above.

FIG. **6**E illustrates a top cross-sectional view of a portion of a semiconductor structure corresponding to the semiconductor structure in FIG. **6**D according to one implementation of the present application. FIG. **6**E represents a cross-sectional view along line "**6**E-**6**E" in FIG. **6**D.

As shown in FIG. **6**E, semiconductor structure **608** includes bulk silicon substrate **620**, porous silicon region **622**, silicon buffer ring **650**, dielectric liner **630**, and TSV **632**. Porous silicon region **622** is situated within bulk silicon substrate **620**, silicon buffer ring **650** is situated within porous silicon region **622**, and TSV **632** is situated within silicon buffer ring **650**. As described above, porous silicon region **622** and silicon buffer ring **650** cause semiconductor structure **608** and/or TSV **632** to withstand thermal and mechanical stresses. As also described above, silicon buffer ring **650** reduces metal diffusion of TSV **632**. Further, because silicon buffer ring **650** is homogeneous single crystal silicon, TSV **632** (and dielectric liner **630** in case dielectric liner **630** is used) are substantially uniform within silicon buffer ring **650**. As used in the present application, the term "buffer ring" is not intended as a limiting shape. In various implementations, silicon buffer ring **650** can have a rectangular shape, or any other shape.

FIG. **6**F illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **510** in the flowchart of FIG. **5** according to one implementation of the present application. As shown in FIG. **6**F, in semiconductor structure **610**, electrical connection layer **638** is formed over TSV **632** and over interlayer dielectric **626**. Electrical connection layer **638** contains at least one electrical connector situated over front end **634** of TSV **632**. Also, electrical connection layer **638** is temporarily bonded with carrier wafer **642** by bonding layer **640**. Except for differences described above, semiconductor structure **610** in FIG. **6**F generally corresponds to semiconductor structure **210** in FIG. **2**F, and may have any implementations and advantages described above.

FIG. **6**G illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **512** the flowchart of FIG. **5** according to one implementation of the present application. As shown in FIG. **6**G, in semiconductor structure **612**, silicon buffer ring **650**, porous silicon regions **622**, and bulk silicon substrate **620** are etched, and back end **636** of TSV **632** is revealed from backside **644** of bulk silicon substrate **620**.

Notably, porous silicon regions **622** are etched to reveal back end **636** of TSV **632**. As a result, porous silicon regions **622** and silicon buffer ring **650** extend substantially to backside **644** of bulk silicon substrate **620**. Accordingly, porous silicon regions **622** and silicon buffer ring **650** greatly improve the ability of semiconductor structure **612** and/or TSV **632** to withstand thermal and mechanical stresses. Except for differences described above, semiconductor structure **612** in FIG. **6**G generally corresponds to semiconductor structure **212** in FIG. **2**G, and may have any implementations and advantages described above.

FIG. **7**A illustrates a cross-sectional view of a portion of a semiconductor structure according to one implementation of the present application. As shown in FIG. **7**A, semiconductor structure **708** includes bulk silicon substrate **720**, porous silicon regions **722**, semiconductor device **724**, interlayer dielectric **726**, dielectric liner **730**, TSV **732**, and

silicon buffer ring **750**. Semiconductor structure **708** represents an implementation employing both a silicon buffer ring and a porous silicon region having a depth less than that of a TSV.

As described above, porous silicon regions **722** and silicon buffer ring **750** cause semiconductor structure **708** and/or TSV **732** to withstand thermal and mechanical stresses. As also described above, silicon buffer ring **750** reduces metal diffusion of TSV **732**. Further, because silicon buffer ring **750** is homogeneous single crystal silicon, TSV **732** (and dielectric liner **730** in case dielectric liner **730** is used) are substantially uniform within silicon buffer ring **750**.

Depth D**7** represents the depth of porous silicon region **722** measured from the top surface of bulk silicon substrate **720**. Depth D**8** represents the depth of TSV **732** (including dielectric liner **730** in case dielectric liner **730** is used) measured from the top surface of bulk silicon substrate **720**. In the present implementation, depth D**7** of porous silicon regions **722** is substantially less than depth D**8** of TSV **732**. Except for differences described above, semiconductor structure **708** in FIG. **7**A generally corresponds to semiconductor structure **608** in FIG. **6**D, and may have any implementations and advantages described above.

FIG. **7**B illustrates a cross-sectional view of a portion of a semiconductor structure corresponding to the semiconductor structure in FIG. **7**A according to one implementation of the present application. As shown in FIG. **7**B, in semiconductor structure **712**, bulk silicon substrate **720** is etched, and back end **736** of TSV **732** is revealed from backside **744** of bulk silicon substrate **720**.

As shown in FIG. **7**A, prior to revealing back end **736** of TSV **732**, the depth of porous silicon regions **722** in bulk silicon substrate **720** was less than the depth of TSV **732** in bulk silicon substrate **720**. In one implementation, the depth of porous silicon regions **722** can be approximately ten microns (10 μm) less than the depth of TSV **732** to ensure that porous silicon regions **722** are not damaged in the reveal action.

As a result, after revealing back end **736** of TSV **732** as shown in FIG. **7**B, porous silicon regions **722** remain substantially unetched. A portion of bulk silicon substrate **720** intervenes between porous silicon regions **722** and backside **744**. Porous silicon regions **722** and silicon buffer ring **750** still improve the ability of semiconductor structure **712** and/or TSV **732** to withstand thermal and mechanical stresses. Moreover, porous silicon regions **722** do not absorb any etching solutions and provide increased reliability. Except for differences described above, semiconductor structure **712** in FIG. **7**B generally corresponds to semiconductor structure **612** in FIG. **6**G, and may have any implementations and advantages described above.

From the above description it is manifest that various techniques can be used for implementing the concepts described in the present application without departing from the scope of those concepts. Moreover, while the concepts have been described with specific reference to certain implementations, a person of ordinary skill in the art would recognize that changes can be made in form and detail without departing from the scope of those concepts. As such, the described implementations are to be considered in all respects as illustrative and not restrictive. It should also be understood that the present application is not limited to the particular implementations described above, but many rearrangements, modifications, and substitutions are possible without departing from the scope of the present disclosure.

The invention claimed is:

1. A semiconductor structure comprising:
- a semiconductor substrate;
- a porous semiconductor region within said semiconductor substrate, wherein said porous semiconductor region is not a dielectric material;
- a through-substrate via (TSV) within said porous semiconductor region;
- said porous semiconductor region causing said semiconductor structure and/or said TSV to withstand thermal and mechanical stresses.

2. The semiconductor structure of claim **1**, wherein said porous semiconductor region has a first coefficient of thermal expansion (CTE) that is significantly greater than a second CTE of said semiconductor substrate.

3. The semiconductor structure of claim **1**, wherein said porous semiconductor region is more deformable than said semiconductor substrate.

4. The semiconductor structure of claim **1**, wherein a first depth of said porous semiconductor region is greater than or equal to a second depth of said TSV.

5. The semiconductor structure of claim **1**, wherein a first depth of said porous semiconductor region is less than a second depth of said TSV.

6. The semiconductor structure of claim **1**, further comprising at least one electrical connector situated over said TSV.

7. The semiconductor structure of claim **1**, wherein said TSV comprises a metal selected from the group consisting of copper (Cu), aluminum (Al), and titanium (Ti).

8. The semiconductor structure of claim **1**, further comprising a dielectric liner between said TSV and said porous semiconductor region.

9. A semiconductor structure comprising:
- a semiconductor substrate;
- a porous semiconductor region within said semiconductor substrate;
- a semiconductor buffer ring within said porous semiconductor region;
- a through-substrate via (TSV) within said semiconductor buffer ring;
- said porous semiconductor region and said semiconductor buffer ring causing said semiconductor structure and/or said TSV to withstand thermal and mechanical stresses.

10. The semiconductor structure of claim **9**, wherein a first depth of said porous semiconductor region is greater than or equal to a second depth of said TSV.

11. The semiconductor structure of claim **9**, wherein a first depth of said porous semiconductor region is less than a second depth of said TSV.

12. The semiconductor structure of claim **9**, further comprising at least one electrical connector situated over said TSV.

13. A semiconductor structure comprising:
- a semiconductor substrate;
- a porous semiconductor region within said semiconductor substrate, wherein said porous semiconductor region is not a dielectric material;
- a through-substrate via (TSV) at least partially within said porous semiconductor region;
- said porous semiconductor region causing said semiconductor structure to withstand thermal or mechanical stress.

14. The semiconductor structure of claim **13**, wherein said porous semiconductor region has a first coefficient of thermal expansion (CTE) that is greater than a second CTE of said semiconductor substrate.

15. The semiconductor structure of claim **13**, wherein said TSV is completely within said porous semiconductor region.

16. The semiconductor structure of claim **13**, wherein said TSV extends beyond said porous semiconductor region.

17. The semiconductor structure of claim **13**, further comprising a dielectric liner between said TSV and said porous semiconductor region.

18. A semiconductor structure comprising:

a semiconductor substrate;

a porous semiconductor region within said semiconductor substrate;

a semiconductor buffer ring within said porous semiconductor region;

a through-substrate via (TSV) at least partially within said semiconductor buffer ring;

said porous semiconductor region or said semiconductor buffer ring causing said semiconductor structure to withstand thermal or mechanical stress.

19. The semiconductor structure of claim **18**, wherein said TSV is completely within said semiconductor buffer ring.

20. The semiconductor structure of claim **18**, wherein said TSV extends beyond said semiconductor buffer ring.

21. The semiconductor structure of claim **18**, further comprising a dielectric liner between said TSV and said semiconductor buffer ring.

* * * * *

Exhibit 5

US 20210375618A1

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(12) **Patent Application Publication**

Hurwitz et al.

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(43) **Pub. Date: Dec. 2, 2021**

(54) **METHOD FOR FORMING A SEMICONDUCTOR STRUCTURE HAVING A POROUS SEMICONDUCTOR LAYER IN RF DEVICES**

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H01L 23/66	(2006.01)
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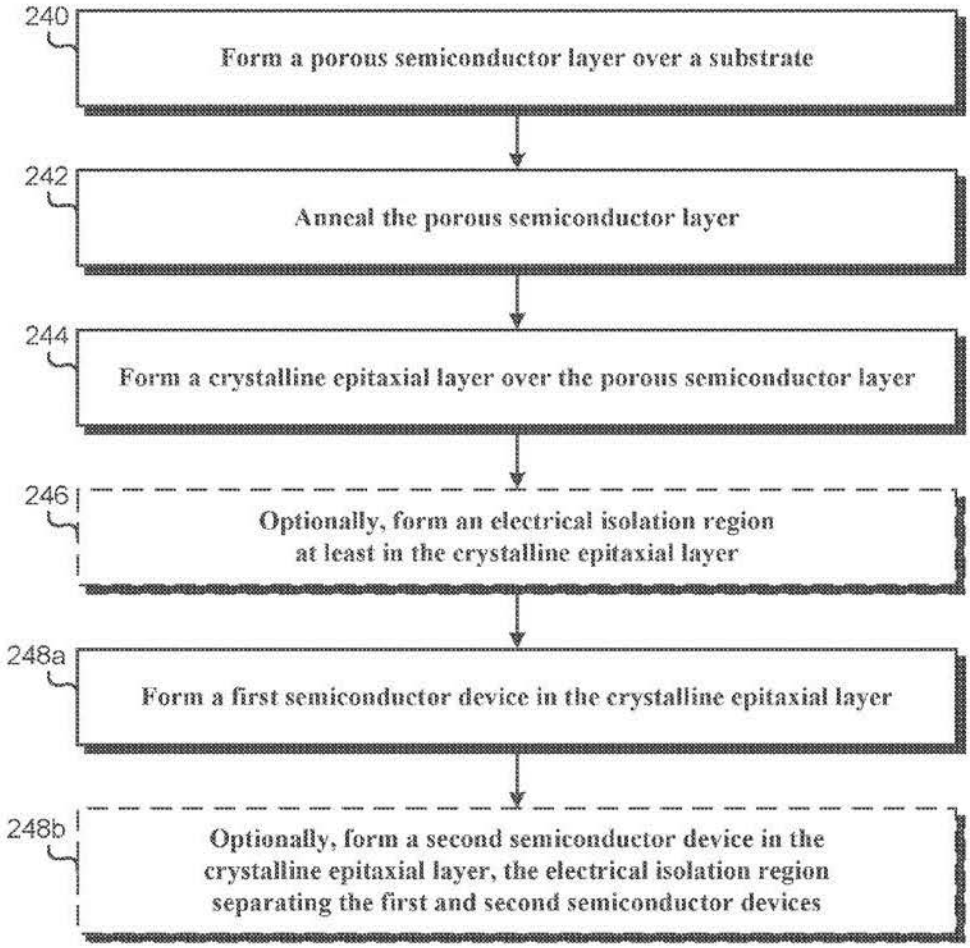
H01L 21/762	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 21/02203*** (2013.01); ***H01L 29/04*** (2013.01); ***H01L 29/0843*** (2013.01); *H01L 2223/6677* (2013.01); ***H03K 17/687*** (2013.01); ***H01L 21/76294*** (2013.01); ***H01L 23/66*** (2013.01)

(57) **ABSTRACT**

A semiconductor structure includes a substrate having a first dielectric constant, a porous semiconductor layer situated over the substrate, and a crystalline epitaxial layer situated over the porous semiconductor layer. A first semiconductor device is situated in the crystalline epitaxial layer. The porous semiconductor layer has a second dielectric constant that is substantially less than the first dielectric constant such that the porous semiconductor layer reduces signal leakage from the first semiconductor device. The semiconductor structure can include a second semiconductor device situated in the crystalline epitaxial layer, and an electrical isolation region separating the first and second semiconductor devices.



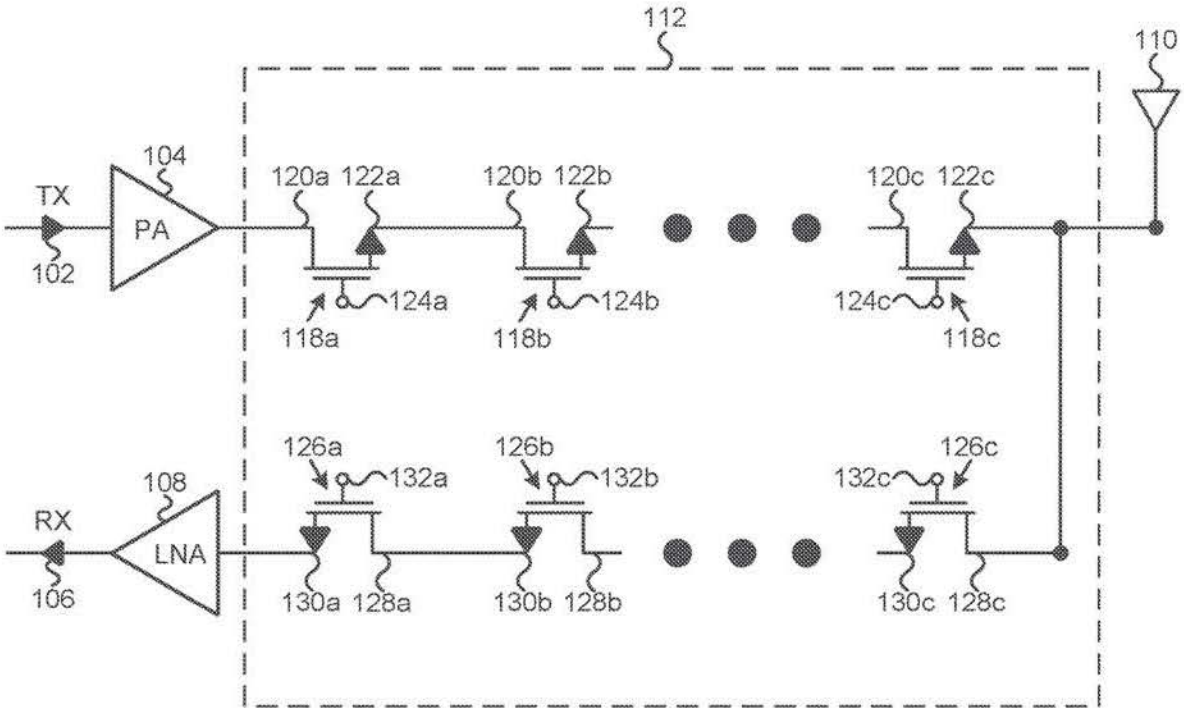

112
110
104
TX
PA
102
120a 122a
120b 122b
120c 122c
124a
124b
124c
118a
118b
118c
126a
126b
126c
132a
132b
132c
108
RX
LNA
106
130a 128a
130b 128b
130c 128c

FIG. 1

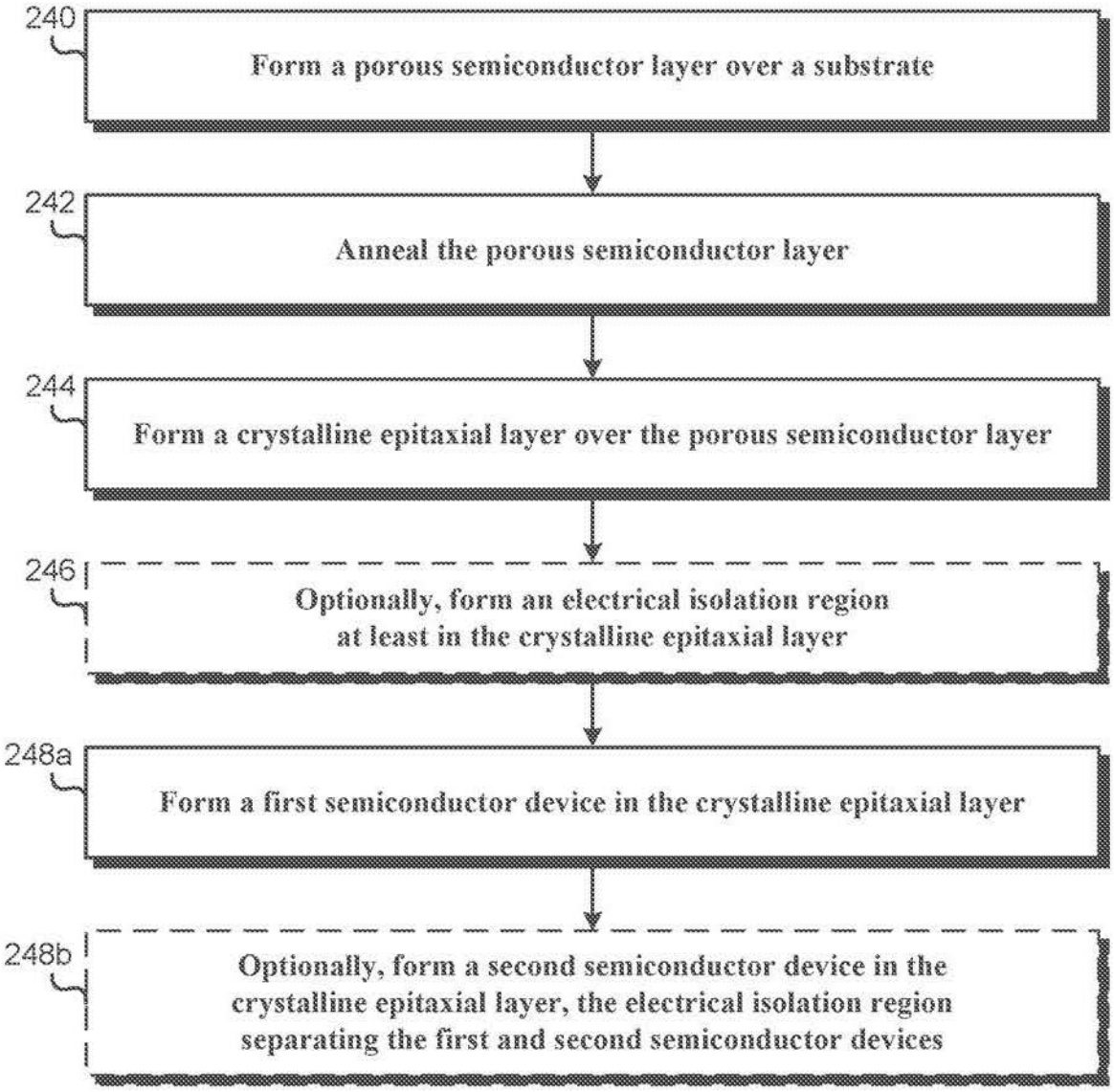

240
Form a porous semiconductor layer over a substrate
242
Anneal the porous semiconductor layer
244
Form a crystalline epitaxial layer over the porous semiconductor layer
246
Optionally, form an electrical isolation region at least in the crystalline epitaxial layer
248a
Form a first semiconductor device in the crystalline epitaxial layer
248b
Optionally, form a second semiconductor device in the crystalline epitaxial layer, the electrical isolation region separating the first and second semiconductor devices

FIG. 2

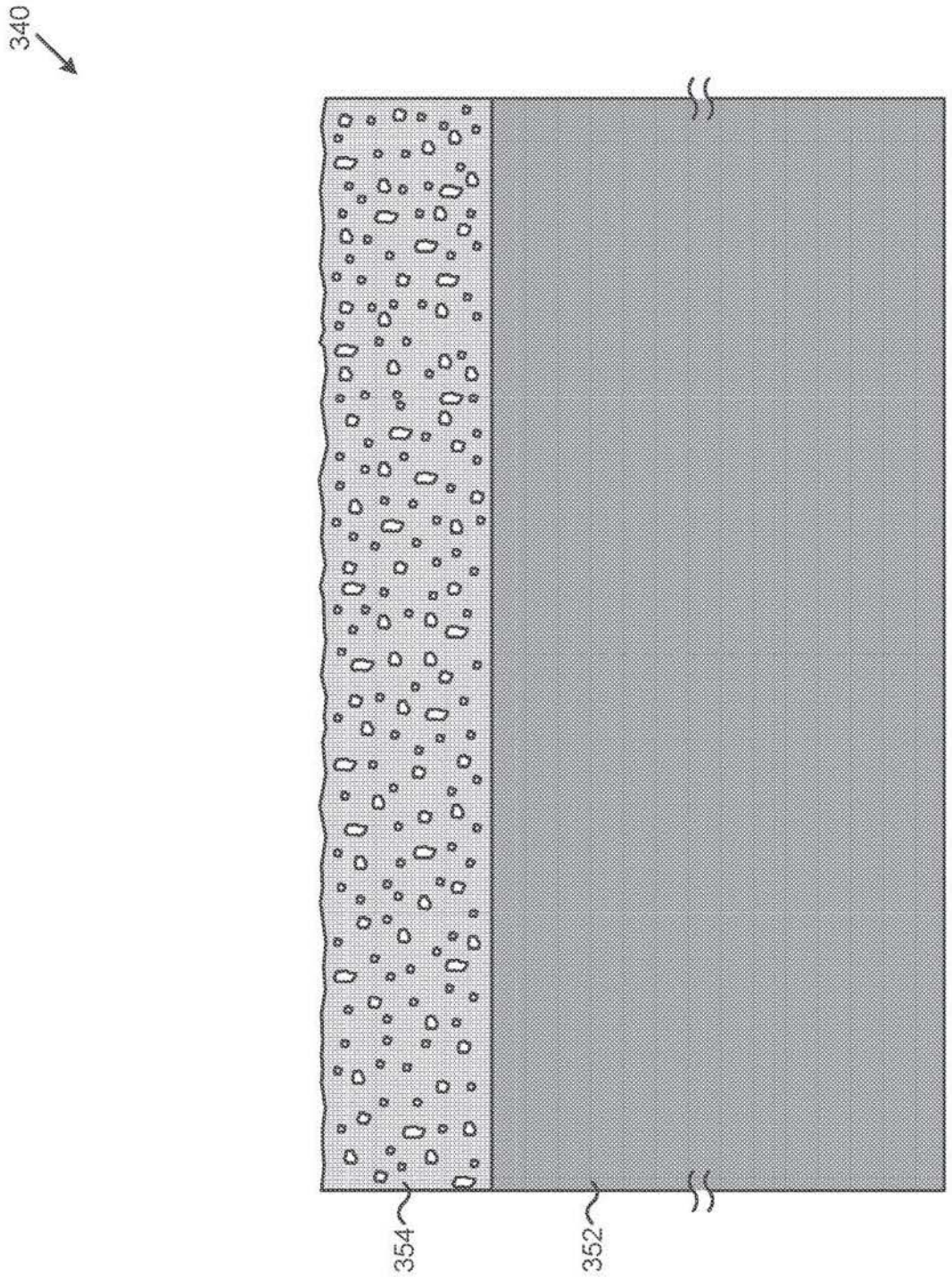


FIG. 3A

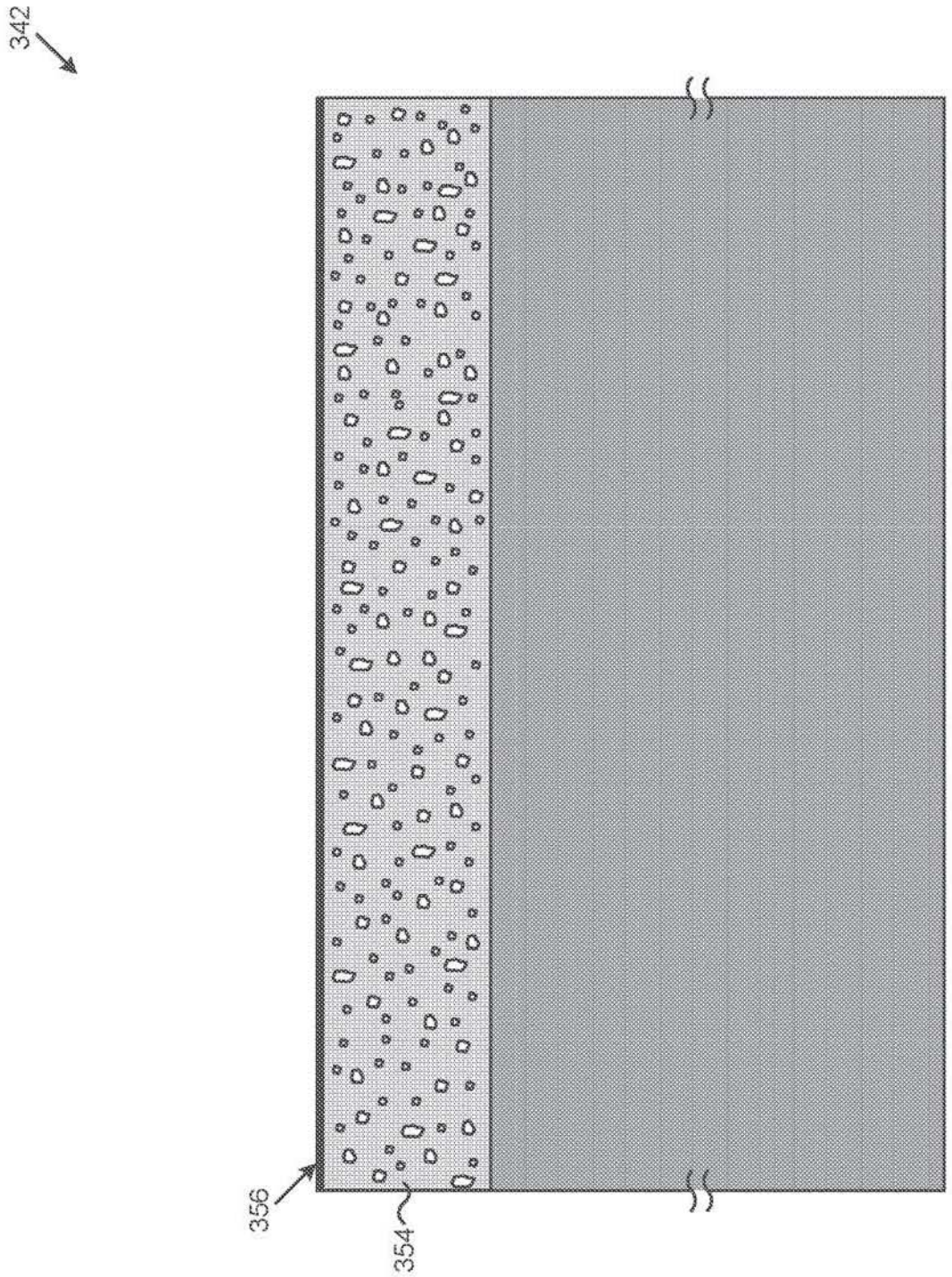


FIG. 3B

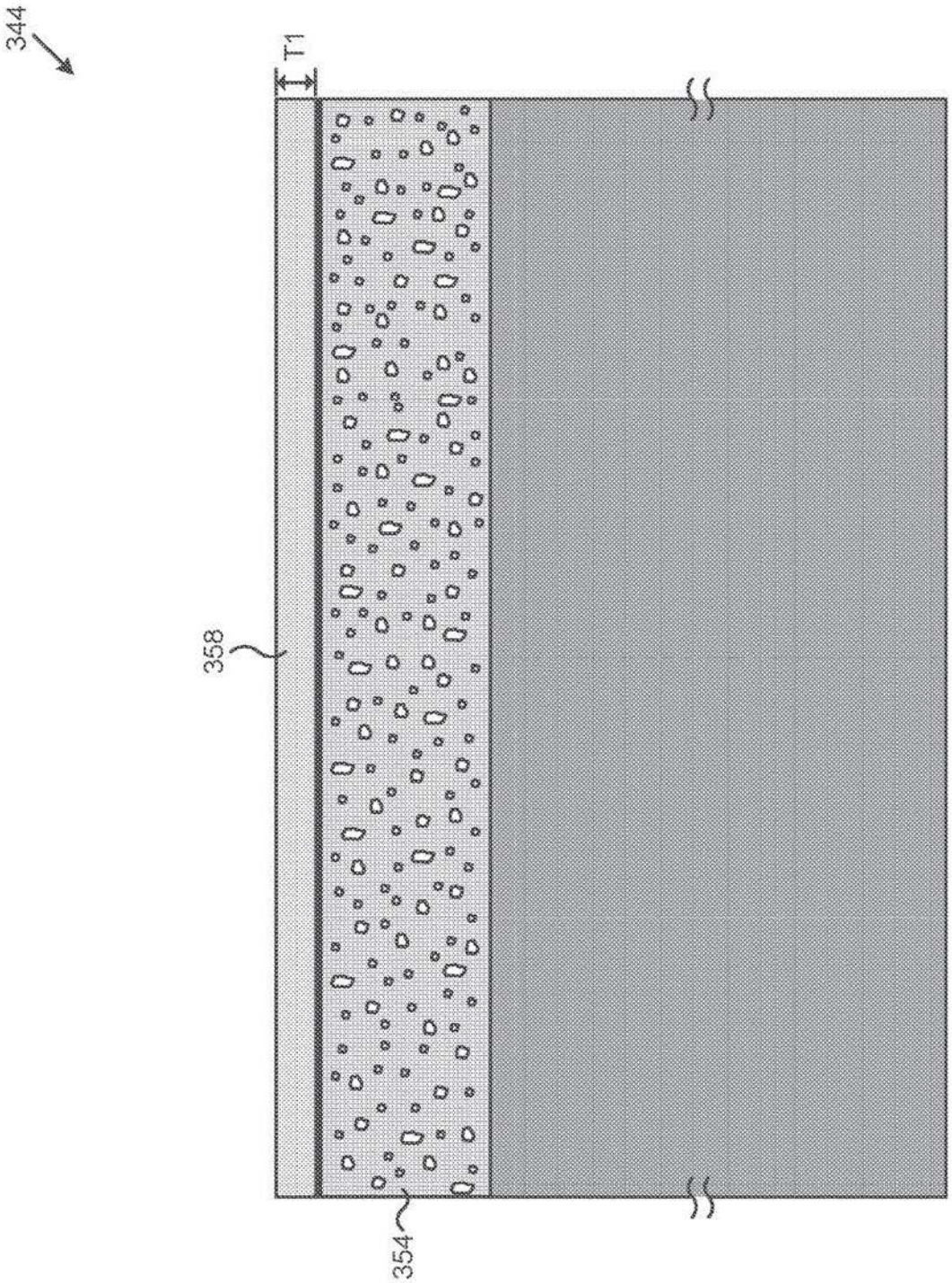


FIG. 3C

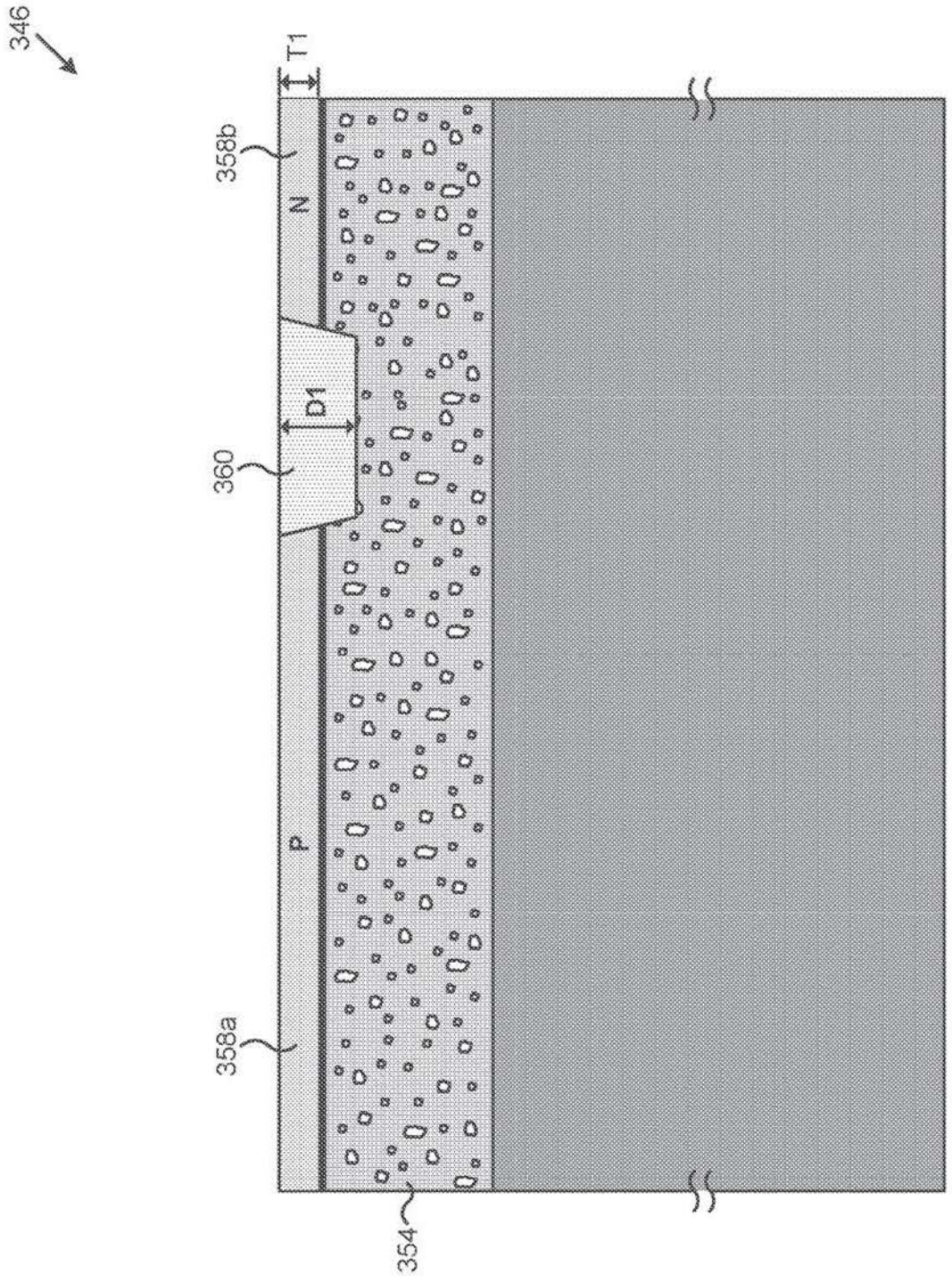


FIG. 3D

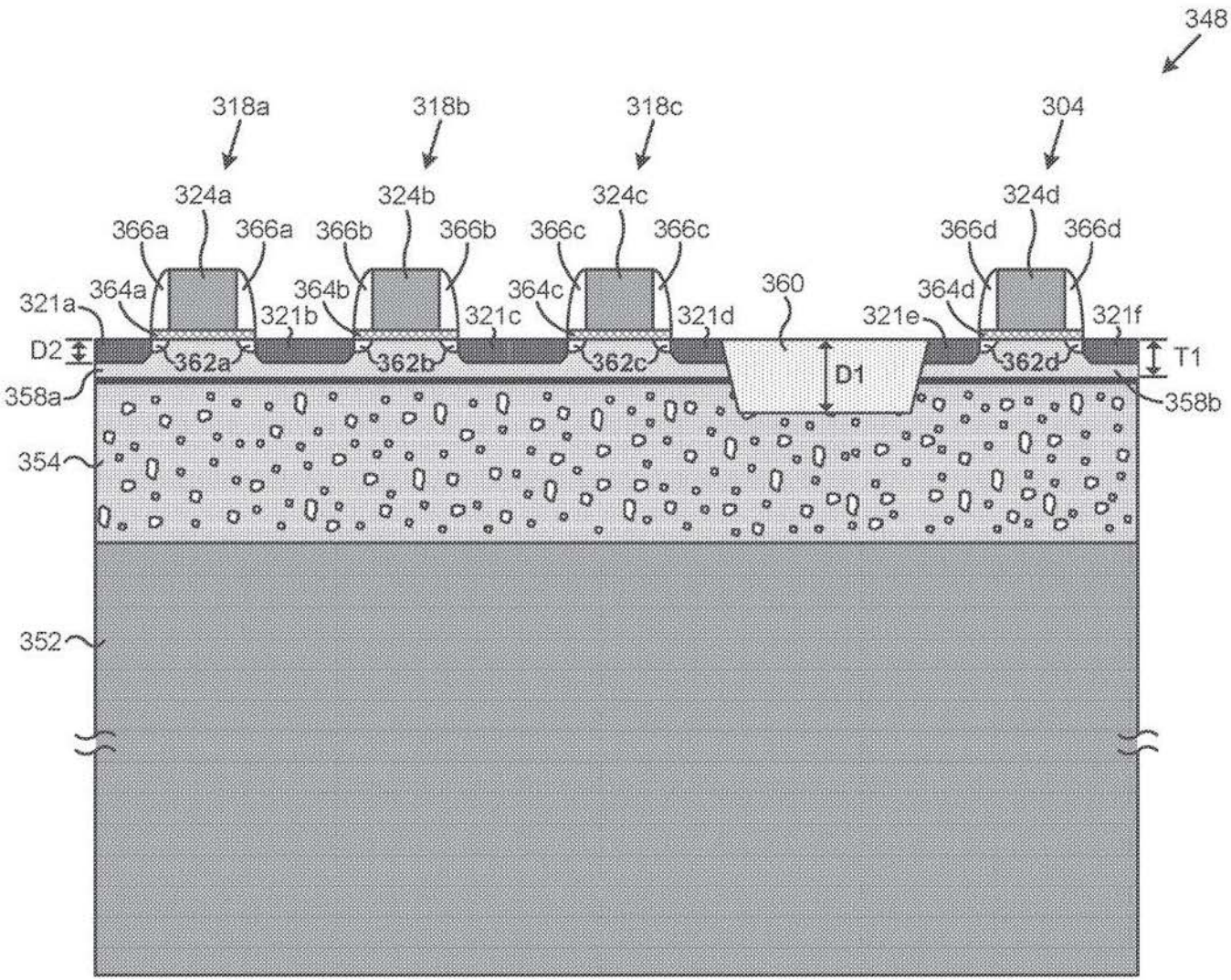

348
318a
318b
318c
304
324a
324b
324c
324d
366a
366a
366b
366b
366c
366c
366d
366d
321a
364a
364b
321b
364c
321c
360
321d
364d
321e
321f
D2
362a
362b
362c
D1
362d
T1
358a
358b
354
352

FIG. 3E

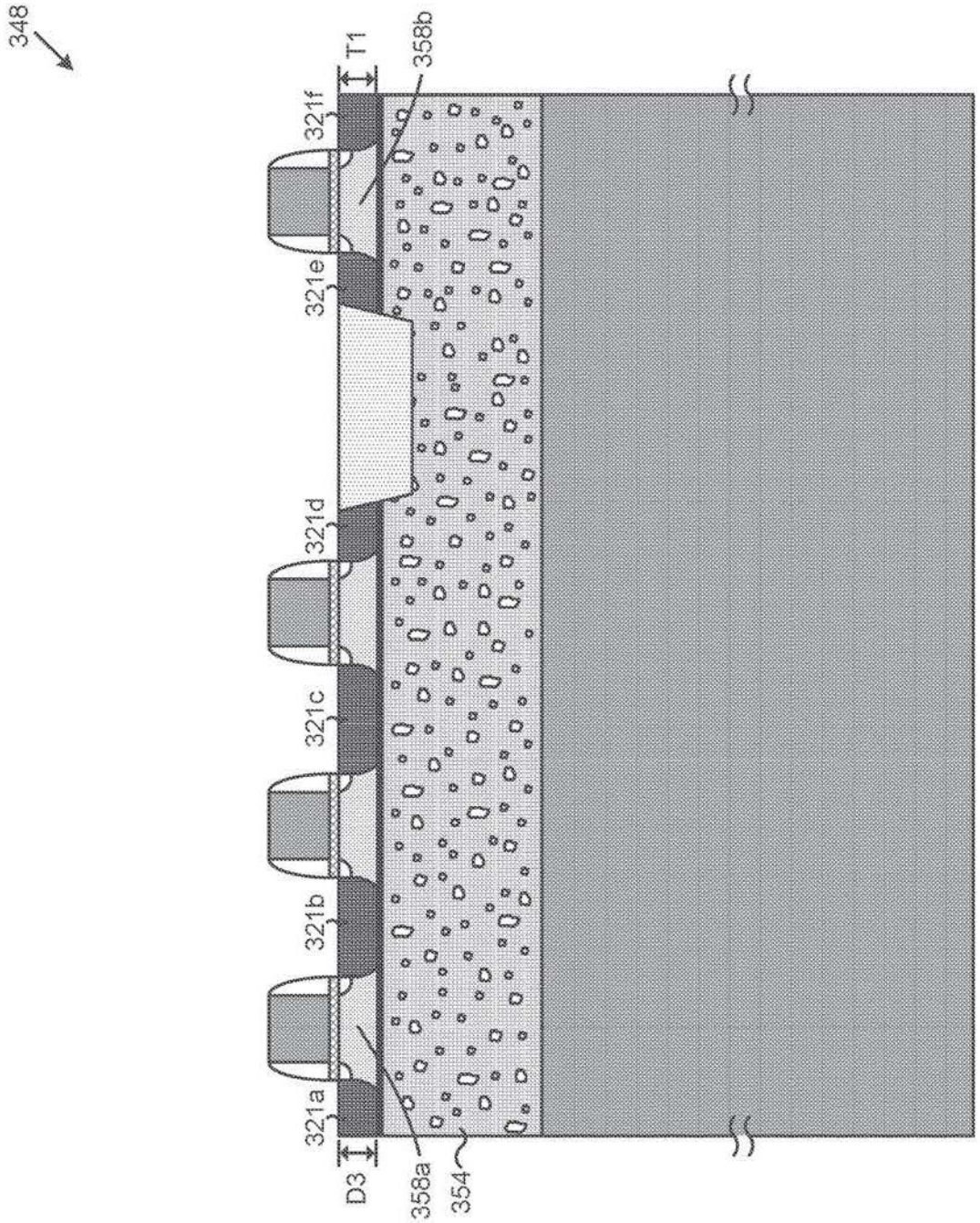


FIG. 3F

METHOD FOR FORMING A SEMICONDUCTOR STRUCTURE HAVING A POROUS SEMICONDUCTOR LAYER IN RF DEVICES

BACKGROUND

[0001] Semiconductor-on-insulator (SOI) structures are commonly employed to realize radio frequency (RF) designs where low signal leakage is required. These SOI structures use a buried oxide (BOX) under a top device layer in which RF circuit components, such as transistors and/or passive components, are fabricated.

[0002] As known in the art, a handle wafer functioning as a. substrate under the BOX results in some signal leakage. In one approach, a high resistivity silicon is used for the handle wafer in order to improve isolation and reduce signal loss. However, the relatively high dielectric constant of silicon (k=11.7) results in significant capacitive loading of RF SOI devices. In another approach, a trap-rich layer is formed between the handle wafer and the BOX in order to minimize parasitic surface conduction effects that would adversely affect RF devices in the top device layer. However, this approach requires costly and/or specialized fabrication techniques.

[0003] Thus, there is need in the art for efficiently and effectively fabricating RF devices with reduced signal leakage at low cost while overcoming the disadvantages and deficiencies of the previously known approaches.

SUMMARY

[0004] The present disclosure is directed to a semiconductor structure having porous semiconductor layer for RF devices, substantially as shown in and/or described in connection with at least one of the figures, and as set forth in the claims,

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. **1** illustrates a portion of a transceiver including a radio frequency (RF) switch employing stacked transistors according to one implementation of the present application.

[0006] FIG. **2** illustrates a portion of a flowchart of an exemplary method for manufacturing a semiconductor structure according to one implementation of the present application.

[0007] FIG. **3**A illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **240** in the flowchart of FIG. **2** according to one implementation of the present application.

[0008] FIG. **3**B illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **242** in the flowchart of FIG. **2** according to one implementation of the present application

[0009] FIG. **3**C illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **244** in the flowchart of FIG. **2** according to one implementation of the present application

[0010] FIG. **3**D illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **246** in the flowchart of FIG. **2** according to one implementation of the present application.

[0011] FIG. **3**E illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with actions **248***a* and **248***b* in the flowchart of FIG. **2** according to one implementation of the present application.

[0012] FIG. **3**F illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with actions **248***a* and **248***b* in the flowchart of FIG. **2** according to one implementation of the present application.

DETAILED DESCRIPTION

[0013] The following description contains specific information pertaining to implementations in the present disclosure. The drawings in the present application and their accompanying detailed description are directed to merely exemplary implementations. Unless noted otherwise, like or corresponding elements among the figures may be indicated by like or corresponding reference numerals. Moreover, the drawings and illustrations in the present application are generally not to scale, and are not intended to correspond to actual relative dimensions.

[0014] FIG. **1** illustrates a portion of a transceiver including a radio frequency (RF) switch employing stacked transistors according to one implementation of the present application. The transceiver in FIG. **1** includes transmit input **102**, power amplifier (PA) **104**, receive output **106**, low-noise amplifier (LNA) **108**, antenna **110**, and radio frequency (RF) switch **112**.

[0015] RF switch **112** is situated between PA **104** and antenna **110**. PA **104** amplifies RF signals transmitted from transmit input **102**. In one implementation, transmit input **102** can be coupled to a mixer (not shown in FIG. **1**), or to another input source. The output of PA **104** is coupled to one end of RF switch **112**. A matching network (not shown in FIG. **1**) can be coupled between PA **104** and RF switch **112**. Another end of RF switch **112** is coupled to antenna **110**. Antenna **110** can transmit amplified RF signals. In one implementation, RF switch **112** can be coupled to an antenna array, rather than a single antenna **110**.

[0016] RF switch **112** is also situated between LNA **108** and antenna **110**. Antenna **110** also receives RF signals. Antenna **110** is coupled to one end of RF switch **112**. Another end of RF switch **112** is coupled to the input of LNA **108**. LNA **108** amplifies RF signals received from RF switch **112**. A matching network (not shown in Figure can be coupled between RF switch **112** and LNA **108**, Receive output **106** receives amplified RF signals from LNA **108**. In one implementation, receive output **106** can be coupled to a mixer (not shown in FIG. **1**), or to another output source.

[0017] RF switch **112** includes two stacks of transistors. The first stack includes transistors **118***a*, **118***b*, and **118***c*. Drain **120***a* of transistor **118***a* is coupled to the output of PA **104**. Source **122***a* of transistor **118***a* is coupled to drain **120***b* of transistor **118***b*. Source **122***b* of transistor **118***b* can be coupled to the drain of additional transistors, and ultimately coupled to drain **120***c* of transistor **118***c*. Source **122***c* of transistor **118***c* is coupled to antenna **110**. Gates **124***a*, **124***b*, and **124***c* of transistors **118***a*, **118***b*, and **118***c* respectively can be coupled to a controller or a pulse generator (not shown) for switching transistors **118***a*, **118***b*, and **118***c* between ON and OFF states.

[0018] The second stack includes transistors **126***a*, **126***b*, and **126***c*. Source **130***a* of transistor **126***a* is coupled to the input of LNA **108**. Drain **128***a* of transistor **126***a* is coupled to source **130***b* of transistor **126***b*. Drain **128***b* of transistor

126*b* can be coupled to the drain of additional transistors, and ultimately coupled to drain source **130***c* of transistor **126***c*. Drain **128***c* of transistor **126***c* is coupled to antenna **110**. Gates **132***a*, **132***b*, and **132***c* of transistors **126***a*, **126***b*, and **126***c* respectively can be coupled to a controller or a pulse generator (not shown) for switching transistors **126***a*, **126***b*, and **126***c* between ON and OFF states.

[0019] In the example of FIG. **1**, RF switch **112** switches the transceiver in FIG. **1** between receive and transmit modes. When transistors **118***a*, **118***b*, and **118***c* are in OFF states, and transistors **126***a*, **126***b*, and **126***c* are in ON states, the transceiver is in receive mode. Transistors **126***a*, **126***b*, and **126***c* serve as a receive path for RF signals received by antenna **110** to pass to INA **108** and to receive output **106**. When transistors **118***a*, **118***b*, and **118***c* are in ON states, and transistors **126***a*, **126***b*, and **126***c* are in OFF states, the transceiver is in transmit mode. Transistors **118***a*, **118***b*, and **118***c* serve as a transmit path for RF signals transmitted from transmit input **102** and PA **104** to pass to antenna **110**. In various implementations, RF switch **112** can include more stacks of transistors and/or more amplifiers. In various implementations, RF switch **112** can switch the transceiver between two transmit modes corresponding to different frequencies, or between two receive modes corresponding to different frequencies.

[0020] In the present implementation, transistors **118***a*, **118***b*, **118***c*, **126***a*, **126***b*, and **126***c* are N-type field effect transistors (NFETs). In various implementations, transistors **118***a*, **118***b*, **118***c*, **126***a*, **126***b*, and **126***c* can be P-type FEB (PFETs), junction FETs (JFETs), or any other type of transistor. By stacking transistors **118***a*, **118***b*, **118***c*, **126***a*, **126***b*, and **126***c* as shown in FIG. **1**, the overall OFF state power and voltage handling capability for RF switch **112** can be increased. For example, if only transistors **118***a* and **126***a* were used, RF switch **112** may have an OFF state voltage handling capability of five volts (5 V). If eight transistors were used in each stack, RF switch **112** may have an OFF state voltage handling capability of forty volts (40 V). In various implementations, RF switch **112** can have more or fewer stacked transistors than shown in FIG. **1**.

[0021] As described below, in conventional semiconductor structures, signals can leak from RF switch **112**, for example, to ground or to other devices. This signal leakage is particularly problematic when transistors **118***a*, **118***b*, **118***c*, **126***a*, **126***b*, and **126***c* are in OFF states, and when dealing with higher frequency signals, such as RF signals. According to the present application, RF switch **112** can be utilized in a semiconductors structure that reduces signal leakage. It is noted that, although the present application focuses on RF signals, the signals pray have frequencies other than RF frequencies.

[0022] FIG. **2** illustrates a portion of a flowchart of an exemplary method for manufacturing a semiconductor structure according to one implementation of the present application. Structures shown in FIGS. **3**A through **3**E illustrate the results of performing actions **240** through **248***b* shown in the flowchart of FIG. **2**. For example, FIG. **3**A shows a semiconductor structure after performing action **240** in FIG. **2**, FIG. **3**B shows a semiconductor structure after performing action **242** in FIG. **2**, and so forth.

[0023] Actions **240** through **248***b* shown in the flowchart of FIG. **2** are sufficient to describe one implementation of the present inventive concepts. Other implementations of the present inventive concepts may utilize actions different from those shown in the flowchart of FIG. **2**. Certain details and features have been left out of the flowchart of FIG. **2** that are apparent to a person of ordinary skill in the art. For example, an action may consist of one or more sub-actions or may involve specialized equipment or materials, as known in the art. Moreover, some actions, such as masking and cleaning actions, are omitted so as not to distract from the illustrated actions.

[0024] FIG. **3**A illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **240** in the flowchart of FIG. **2** according to one implementation of the present application. As shown FIG. **3**A, according to action **240**, semiconductor structure **340** including porous semiconductor layer **354** situated over substrate **352** is formed. In the present implementation, substrate **352** is a bulk silicon substrate. For example, substrate **352** can be a P-type bulk silicon substrate having a thickness of approximately seven hundred microns (700 μm). In various implementations, substrate **352** may be any other type of substrate.

[0025] Porous semiconductor layer **354** situated over substrate **352** is a semiconductor layer having voids, or pores, therein, Within porous semiconductor layer **354**, the pores can have any orientation, branching, fill, or other morphological characteristic known in the art. Porous semiconductor layer **354** can be formed by using a top-down technique, where portions of substrate **352** are removed to generate pores. For example, porous semiconductor layer **354** can be formed by electrochemical etching using hydrofluoric acid (HF). Alternatively, porous semiconductor layer **354** can also be formed by stain etching, photoetching, or any other top-down technique known in the art. Porous semiconductor layer **354** can also be formed by using a bottom-up technique, where deposition results in a semiconductor layer having empty spaces. For example, porous semiconductor layer **354** can be formed by low-temperature high-density plasma (HDP) deposition. Alternatively, porous semiconductor layer **354** can also be formed by plasma hydrogenation of an amorphous layer, laser ablation, or any other bottom-up technique known in the art. In the present implementation, porous semiconductor layer **354** is a porous silicon layer, and has a thickness from approximately ten microns (10 μm) to approximately fifty microns (50 μm). In various implementations, porous semiconductor layer **354** may be any other type of porous semiconductor layer.

[0026] FIG. **3**B illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **242** in the flowchart of FIG. **2** according to one implementation of the present application. In semiconductor structure **342**, porous semiconductor layer **354** is annealed. For example, porous semiconductor layer **354** can be annealed in argon (Ar) or hydrogen (H_2) at atmospheric pressure from a temperature of approximately seven hundred degrees Celsius (700° C.) to a temperature of approximately eleven hundred degrees Celsius (1100° C.) for approximately ten minutes (10 min). Any other annealing technique known in the art can be utilized, such as techniques utilizing different temperatures, durations, and/or pressures. The annealing shown in FIG. **3**B reorganizes the pores in porous semiconductor layer **354** into larger cavities, while closing and smoothing surface **356** of porous semiconductor layer **354**. The annealed porous semiconductor layer **354** serves as a template layer for growth of a crystalline epitaxial layer in a subsequent action.

[0027] FIG. **3**C illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with action **244** in the flowchart of FIG. **2** according to one implementation of the present application. In semiconductor structure **344**, crystalline epitaxial layer **358** is formed over porous semiconductor layer **354**. Crystalline epitaxial layer **358** is a thin layer of single-crystal material situated over porous semiconductor layer **354**. In one implementation, crystalline epitaxial layer **358** is formed by chemical vapor deposition (CVD). In various implementations, crystalline epitaxial layer **358** can be formed by any other epitaxy technique known the art. In the present implementation, crystalline epitaxial layer **358** is a silicon epitaxial layer, and has thickness T**1** from approximately five hundred angstroms (500 Å) to approximately two thousand angstroms (2000 Å). In various implementations, crystalline epitaxial layer **358** may be any other type of crystalline epitaxial layer. In various implementations, more than one crystalline epitaxial layer **358** can be formed. Crystalline epitaxial layer **358** serves as device region for formation of semiconductor devices in subsequent actions.

[0028] FIG. **3**D illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with optional action **246** in the flowchart of FIG. **2** according to one implementation of the present application. In semiconductor structure **346** of FIG. **3**D, electrical isolation region **360** is formed at least in crystalline epitaxial layer **358** (shown in FIG. **3**C). In particular, in the example of FIG. **3**D, electrical isolation region **360** extends through crystalline epitaxial layer **358** and into porous semiconductor layer **354**.

[0029] Electrical isolation region **360** can be formed by etching through crystalline epitaxial layer **358** and into porous semiconductor layer **354**, then depositing an electrically insulating material. In the present implementation, electrical isolation region **360** is also planarized with the top surface of crystalline epitaxial layer **358**, for example, by using chemical machine polishing (CMP). Electrical isolation on **360** can comprise, for example, silicon dioxide (SiO_2).

[0030] In the present implementation, depth D**1** of electrical isolation region **360** is greater than thickness T**1** of crystalline epitaxial layer **358**. Accordingly, electrical isolation region **360** separates crystalline epitaxial layer **358** of FIG. **3**C into two crystalline epitaxial layers **358***a* and **358***b*. In one implementation, depth D**1** of electrical isolation region **360** can be substantially equal to thickness T**1**. In another implementation, depth D**1** of electrical isolation region **360** can be less than thickness T**1**, such that electrical isolation region **360** extends into crystalline epitaxial layer **358** but not into porous semiconductor layer **354**. In various implementations, locally oxidized silicon (LOCOS) can be used instead of or in addition to electrical isolation region **360**.

[0031] Crystalline epitaxial layers **358***a* and **358***b* can also be implanted with a dopant. For example, crystalline epitaxial layers **358***a* and **358***b* can be implanted with boron or other appropriate P-type dopant. In another example, one or both of crystalline epitaxial layers **358***a* and **358***b* can be implanted with phosphorus or other appropriate N-type dopant. One or more masks can be utilized to define portions of crystalline epitaxial layers **358***a* **358***b* that will be implanted with dopants. In one implementation, crystalline epitaxial layers **358***a* and **358***b* are implanted with a dopant after forming electrical isolation region **360**. In another implementation, crystalline epitaxial layer **358** in FIG. **3**C can be implanted with dopants before forming electrical isolation region **360**. In this implementation, electrical isolation region **360** can be formed in a uniform implant region, between two implant regions having different types or concentrations, and/or where two implant regions overlap.

[0032] As described below, electrical isolation region **360** reduces signal interference across crystalline epitaxial layers **358***a* and **358***b*. Electrical isolation region **360** is considered optional in that semiconductor structures according to the present application can be formed without electrical isolation region **360**.

[0033] FIG. **3**E illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with actions **248***a* and **248***b* in the flowchart of FIG. **2** according to one implementation of the present application. In semiconductor structure **348** of FIG. **3**E, semiconductor devices **318***a*, **318***b*, and **318***c* are formed in crystalline epitaxial layer **358***a*. Similarly, semiconductor device **304** is formed in crystalline epitaxial layer **358***b*. Electrical isolation region **360** separates semiconductor device **304** from semiconductor devices **318***a*, **318***b*, and **318***c*.

[0034] In the present implementation, semiconductor devices **318***a*, **318***b*, and **318***c* are transistors. Semiconductor devices **318***a*, **318***b*, and **318***c* in FIG. **3**E may generally correspond to transistors **118***a*, **118***b*, and **118***c* (or transistors **126***a*, **126***b*, and **126***c*) utilized in RF switch **112** in FIG. **1**. Semiconductor device **318***a* includes source/drain junctions **321***a* and **321***b*, gate **324***a*, lightly doped regions **362***a*, gate oxide **364***a*, and spacers **366***a*. Semiconductor device **318***b* includes source/drain junctions **321***b* and **321***c*, gate **324***b*, lightly doped regions **362***b*, gate oxide **364***b*, and spacers **366***b*. Semiconductor device **318***c* includes source/drain junctions **321***c* and **321***d*, gate **324***c*, lightly doped regions **362***c*, gate oxide **364***c*, and spacers **366***c*. Source/drain junction **321***b* is shared by semiconductor devices **318***a* and **318***b*; source/drain junction **321***c* is shared by semiconductor devices **318***b* and **318***c*.

[0035] In the present implementation, semiconductor device **304** is also a transistor. Semiconductor device **304** in FIG. **3**E can be utilized in an amplifier, such as PA **104** (or LNA **108**) in FIG. **1**. Semiconductor device **304** includes source/drain junctions **321***e* and **321***f*, gate **324***d*, lightly doped regions **362***d*, gate oxide **364***d*, and spacers **366***d*. In one implementation, semiconductor device **304** can be utilized as part of a logic circuit. Semiconductor device **304** is considered optional in that semiconductor structures according to the present application can be formed without semiconductor device **304**.

[0036] Gates **324***a*, **324***b*, **324***e*, and **324***d* can comprise, for example, polycrystalline silicon (polySi). Source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* can be implanted with a dopant of a different type than their corresponding crystalline epitaxial layer **358***a* or **358***b*. Lightly doped regions **362***a*, **362***b*, **362***c*, and **362***d* can be implanted with a dopant of the same type as their adjacent source/drain junction, but having a lower concentration. Gate oxides **364***a*, **364***b*, **364***c*, and **364***d* can comprise, for example, silicon dioxide (SiO_2). Spacers **366***a*, **366***b*, **366***c*, and **366***d* can comprise, for example, silicon nitride (SiN).

[0037] In the present implementation, depth D**2** of source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* is substantially less than thickness T**1** of crystalline epitaxial

layers **358***a* and **358***b*, such that source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* are not in contact with porous semiconductor layer **354**. In one implementation, source/drain junctions **321***a*, **321***b*, **321***c*, and **321***d* are implanted with an N-type dopant (or a P-type dopant in some implementations) in one action, and source/drain junctions **321***e* and **321***f* are implanted with an N-type dopant (or a P-type dopant in some implementations) another separate action. In one implementation, source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* are implanted with an N-type dopant (or a P-type dopant in some implementations) concurrently in a single action. In various implementations, silicide can be situated over source/drain junctions **321***a*, **321***b*, **321***c*, and **321***d* and/or gates **324***a*, **324***b*, and **324***c*. In various implementations, semiconductor structure **348** can include more or fewer semiconductor devices in crystalline epitaxial layer **358***a*. In various implementations, crystalline epitaxial layers **358***a* and **358***b* can include diodes, or types of semiconductor devices instead of or in addition to transistors.

[0038] Because semiconductor structure **348** includes porous semiconductor layer **354** (for example, a porous silicon layer), semiconductor structure **348** reduces signal leakage (for example, RF signal leakage) from semiconductor devices **318***a*, **318***b*, **318***c*, and **304** to ground. Further, porous semiconductor layer **354** (for example, a porous silicon layer) reduces signal interference (for example, RF signal interference) between the different devices built in crystalline epitaxial layers **358***a* and **358***b*. Pores in porous semiconductor layer **354** decrease its effective dielectric constant and increase its resistivity. In semiconductor structure **348** in FIG. **3**E, porous semiconductor layer **354** has a dielectric constant substantially less than the dielectric constant of substrate **352**. For example, when substrate **352** is a bulk silicon substrate having a dielectric constant of approximately 11.7, porous semiconductor layer **354** has a dielectric constant significantly less than 11.7. In particular, porous semiconductor layer **354** can have a dielectric constant from approximately 2.0 to approximately 4.0. The improved RF isolation that results from the low dielectric constant is especially advantageous for RF switching applications as it reduces signal distortion (i.e. improves linearity). It also results in a more uniform voltage distribution across the OFF state FET stack, increasing its power handling capability.

[0039] In semiconductor structure **348** in FIG. **3**E, utilizing porous semiconductor layer **354**, with its low dielectric constant, reduces parasitic capacitance between crystalline epitaxial layer **358***a* and substrate **352**. Accordingly, RF signals are less likely to leak from semiconductor devices **318***a*, **318***b*, and **318***c* in crystalline epitaxial layer **358***a* to substrate **352**. For example, in one implementation, semiconductor devices **318***a*, **318***b*, and **318***c* are transistors utilized to maintain RF switch **112** (shown in FIG. **1**) in an OFF state, and substrate **352** functions as a ground. In their OFF states, transistors **318***a*, **318***b*, and **318***c* create a high resistance path along source/drain junctions **321***a*, **321***b*, **321***c*, and **321***d*, while the RF signals would have been subject to adverse impact of parasitic capacitances with substrate **352** if porous semiconductor layer **354** were not utilized. In other words, the RF signals could easily leak from semiconductor devices **318***a*, **318***b*, and **318***c* to ground, increasing OFF state parasitic capacitance and negatively impacting the performance of semiconductor structure **348**. Where semiconductor devices **318***a*, **318***b*, and **318***c* are transistors utilized to maintain RF switch **112** (shown in FIG. **1**) in an ON state, RF signal leakage, absent porous semiconductor layer **354**, could. also result in a higher insertion loss.

[0040] Because semiconductor structure **348** includes porous semiconductor layer **354** in combination with electrical isolation region **360**, semiconductor structure **348** also reduces signal interference from semiconductor devices **318***a*, **318***b*, **318***c* to semiconductor device **304**, and vice versa. If porous semiconductor layer **354** and electrical isolation region **360** were not utilized, signals (for example RF signals) from semiconductor device **304** could propagate through crystalline epitaxial layers **358***b* and **358***a* and/or substrate **352**, and interfere with semiconductor devices **318***a*, **318***b*, **318***c* and generate additional undesirable noise in semiconductor devices **318***a*, **318***b*, **318***c*. Where semiconductor device **304** is a transistor utilized in PA **104** (shown in FIG. **1**), these consequences could be amplified. Together, the low dielectric constant of porous semiconductor layer **354** and electrical insulation of electrical isolation region **360** reduce signal leakage and interference through crystalline epitaxial layers **358***a* and **358***b* and/or substrate **352**. The leakage and interference are especially reduced where depth D**1** of electrical isolation region **360** is equal to or greater than thickness T**1** of crystalline epitaxial layers **358***a* and **358***b*.

[0041] Semiconductor structure **348** in FIG. **3**E can achieve this reduced signal leakage without using costly materials for substrate **352**, such as quartz or sapphire, and also without requiring costly and/or specialized fabrication techniques used to create trap-rich silicon-on-insulator (SOI) structures, such as smart cut techniques. As described above porous semiconductor layer **354** (for example, a porous silicon layer) can have a dielectric constant from approximately 2.0 to approximately 4.0, comparable to a buried oxide (BOX) in an SOI structure having a dielectric constant of approximately 3.7. Porous semiconductor layer **354** (for example, a porous silicon layer) can be situated over bulk semiconductor substrate **352** (for example, a bulk silicon substrate), and included in semiconductor structure **348** by various fabrication techniques. Thereafter, as discussed above, porous semiconductor layer **354** can be annealed and serve as a high-quality template for growth of crystalline epitaxial layer **358** (shown in FIG. **3**C), in which semiconductor devices **318***a*, **318***b*, **318***c*, and **304** are formed. Further, shallow source/drain junctions **321***a*, **321***b*, **321***c*, and **321***d* improve performance of semiconductor devices **318***a*, **318***b*, and **318***c* by reducing junction capacitances.

[0042] FIG. **3**F illustrates a cross-sectional view of a portion of a semiconductor structure processed in accordance with actions **248***a* and **248***b* in the flowchart of FIG. **2** according to cone implementation of the present application. Semiconductor structure **348** of FIG. **3**F represents an alternative implementation to semiconductor structure **348** of FIG. **3**E. Semiconductor structure **348** of FIG. **3**F is similar to semiconductor structure **348** of FIG. **3**E, except that, in semiconductor structure **348** of FIG. **3**F, depth D**3** of source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* is substantially equal to thickness T**1** of crystalline epitaxial layers **358***a* and **358***b*, such that source/drain junctions **321***a*, **321***b*, **321***c*, **321***d*, **321***e*, and **321***f* are in contact with porous semiconductor layer **354**. Compared to semi-

conductor structure **348** of FIG. **3**E, deeper source/drain junctions **321***e* and **321***f* in semiconductor structure **348** of FIG. **3**F improve performance of semiconductor device **304** by improving high current and high voltage handling. Other than the differences described above, semiconductor structure **348** of FIG. **3**F may have any implementations and advantages described above with respect to semiconductor structure **348** of FIG. **3**E.

[0043] From the above description it is manifest that various techniques can be used for implementing the concepts described in the present application without departing from the scope of those concepts. Moreover, while the concepts have been described with specific reference to certain implementations, a person of ordinary skill in the art would recognize that changes can be made in form and detail without departing from the scope of those concepts. As such, the described implementations are to be considered in all respects as illustrative and not restrictive. It should also be understood that the present application is not limited to the particular implementations described above, but many rearrangements, modifications, and substitutions are possible without departing from the scope of the present disclosure.

1-13. (canceled)

14. A method comprising:

forming a crystalline epitaxial layer over a porous semiconductor layer, said porous semiconductor layer being situated over a substrate;

forming a first semiconductor device in said crystalline epitaxial layer;

said substrate having a first dielectric constant, and said porous semiconductor layer having a. second dielectric constant that is substantially less than said first dielectric constant such that said porous semiconductor layer reduces signal leakage from said first semiconductor device.

15. The method of claim **14**, further comprising annealing said porous semiconductor layer prior to said forming said crystalline epitaxial layer.

16. The method of claim **14**, further comprising forming an electrical isolation region at least in said crystalline epitaxial layer.

17. The method of claim **16**, wherein a depth of said electrical isolation region is equal to or greater than a thickness of said crystalline epitaxial layer.

18. The method of claim **16**, further comprising forming a second semiconductor device in said crystalline epitaxial layer, wherein said electrical isolation region separates said first and second semiconductor devices.

19. The method of claim **14**, wherein said first semiconductor device is a transistor utilized in a radio frequency (RF) switch.

20. The method of claim **19**, wherein a depth of a source/drain junction of said transistor is substantially less than a thickness of said crystalline epitaxial layer, such that said source/drain junction is not in contact with said porous semiconductor layer.

21. The method of claim **19**, wherein a depth of a source/drain junction of said transistor is substantially equal to a thickness of said crystalline epitaxial layer, such that said source/drain junction is in contact with said porous semiconductor layer.

22. A method comprising:

forming at least one crystalline epitaxial layer over a porous silicon layer in a semiconductor structure;

forming first and second transistors and an electrical isolation region separating said first and second transistors in said at least one crystalline epitaxial layer.

23. The method of claim **22**, further comprising forming said porous silicon layer over a bulk silicon substrate prior to said forming said at least one crystalline epitaxial layer.

24. The method of claim **22**, wherein a depth of said electrical isolation region is equal to or greater than a thickness of said at least one crystalline epitaxial layer.

25. The method of claim **22**, wherein a depth of a source/drain junction of said first transistor is substantially less than a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is not in contact with said porous silicon layer.

26. The method of claim **22**, wherein a depth of a source/drain junction of said first transistor is substantially equal to a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is in contact with said porous silicon layer.

27. A method comprising:

forming a porous semiconductor layer over a substrate, said porous semiconductor layer having a higher resistivity than said substrate;

forming at least one crystalline epitaxial layer over said porous semiconductor layer;

forming a first semiconductor device in said at least one crystalline epitaxial layer.

28. The method of claim **27**, wherein said substrate comprises a first semiconductor material, and said porous semiconductor layer comprises said first semiconductor material.

29. The method of claim **27**, wherein said substrate comprises a first semiconductor material, and said porous semiconductor layer comprises a second semiconductor material.

30. The method of claim **27**, further comprising forming a second semiconductor device and an electrical isolation region separating said first and second semiconductor devices in said at least one crystalline epitaxial layer.

31. The method of claim **30**, wherein a depth of said electrical isolation region is equal to or greater than a thickness of said at least one crystalline epitaxial layer.

32. The method of claim **27**, wherein said first semiconductor device is a transistor utilized in a radio frequency (RF) switch.

33. The method of claim **32**, wherein a depth of a source/drain junction of said transistor is substantially less than a thickness of said at least one crystalline epitaxial layer, such that said source/drain junction is not in contact with said porous semiconductor layer.

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Exhibit 6

[Provisionally Filed Under Seal in its Entirety]

Exhibit 7

[Provisionally Filed Under Seal in its Entirety]

Exhibit 8

[Provisionally Filed Under Seal in its Entirety]

Exhibit 9

[Provisionally Filed Under Seal in its Entirety]

Exhibit 10

[Provisionally Filed Under Seal in its Entirety]

Exhibit 11

[Provisionally Filed Under Seal in its Entirety]