POWER10 Processor Chip

Technology and Packaging:

- 602mm^2 7nm Samsung (18B devices)
- 18 layer metal stack, enhanced device
- Single-chip or Dual-chip sockets

Computational Capabilities:

- Up to 15 SMT8 Cores (2 MB L2 Cache / core)
  (Up to 120 simultaneous hardware threads)
- Up to 120 MB L3 cache (low latency NUCA mgmt)
- 3x energy efficiency relative to POWER9
- Enterprise thread strength optimizations
- AI and security focused ISA additions
- 2x general, 4x matrix SIMD relative to POWER9
- EA-tagged L1 cache, 4x MMU relative to POWER9

Open Memory Interface:

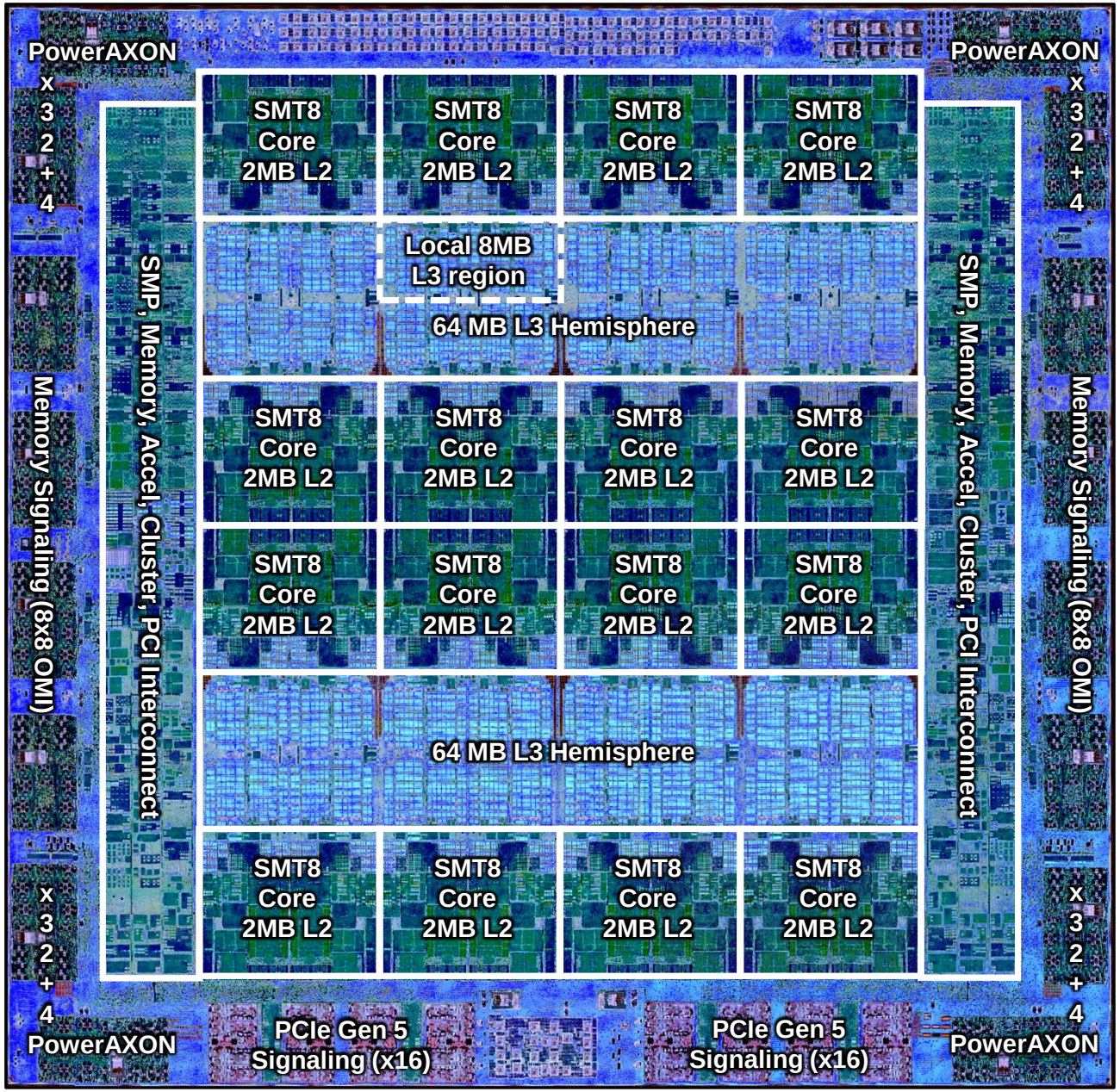
- 16 x8 at up to 32 GT/s (1 TB/s)
- Technology agnostic support: near/main/storage tiers
- Minimal (< 10ns latency) add vs DDR direct attach

PowerAXON Interface:

- 16 x8 at up to 32 GT/s (1 TB/s)
- SMP interconnect for up to 16 sockets
- OpenCAPI attach for memory, accelerators, I/O
- Integrated clustering (memory semantics)

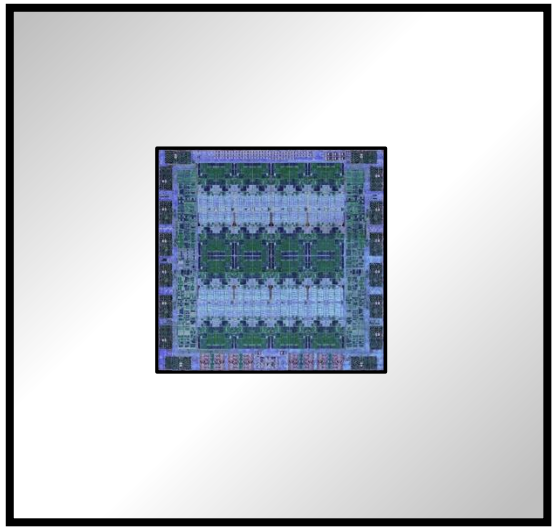
PCIe Gen 5 Interface:

- x64 / DCM at up to 32 GT/s



Die Photo courtesy of Samsung Foundry

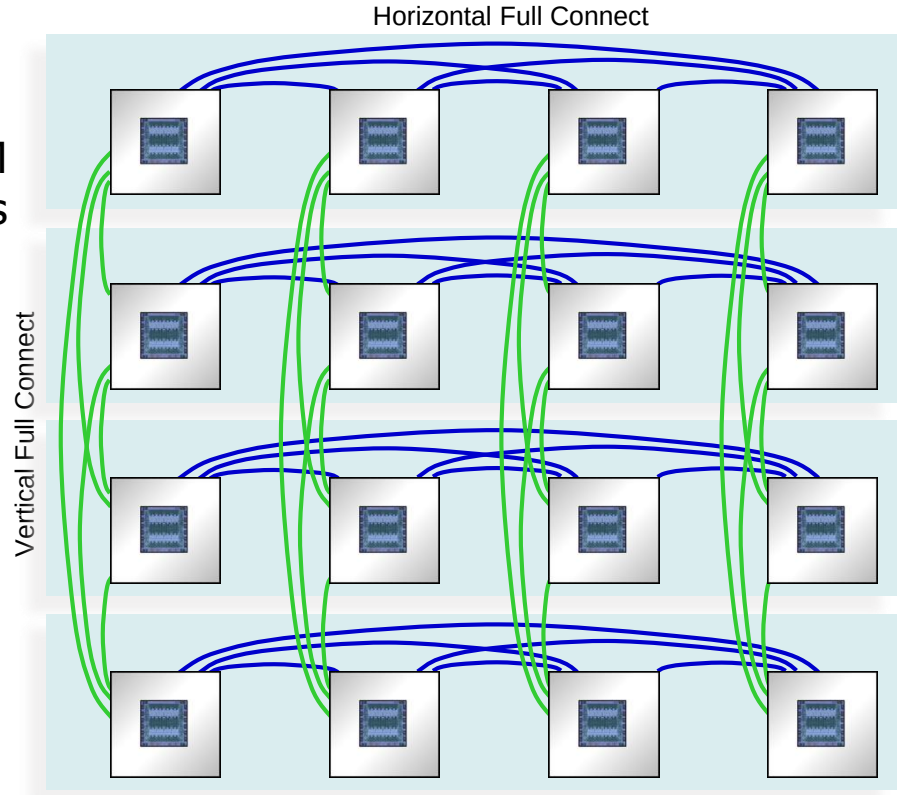
Socket Composability: SCM & DCM

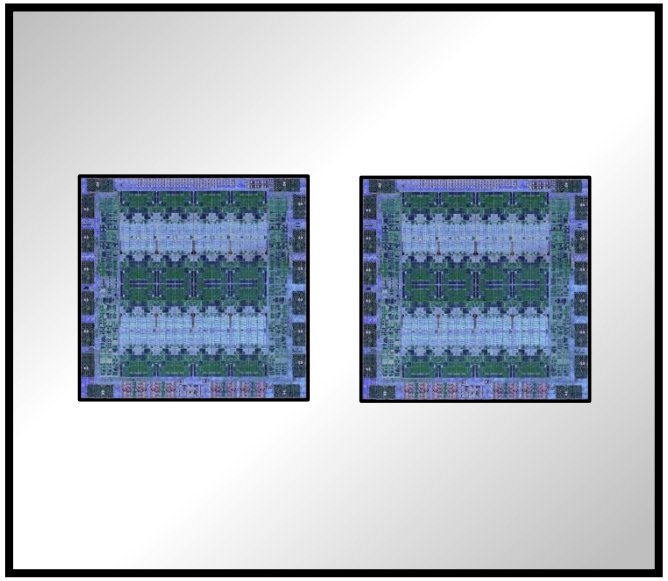


Single-Chip Module Focus:

- 602mm^2 7nm (18B devices)
- Core/thread Strength
  - Up to 15 SMT8 Cores (4+ GHz)
- Capacity & Bandwidth / Compute
  - Memory: x128 @ 32 GT/s
  - SMP/Cluster/Accel: x128 @ 32 GT/s
  - I/O: x32 PCIe G5
- System Scale (Broad Range)
  - 1 to 16 sockets

Up to 16 SCM Sockets

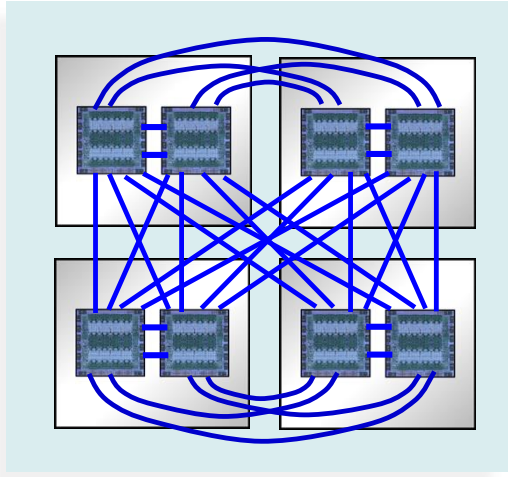




Dual-Chip Module Focus:

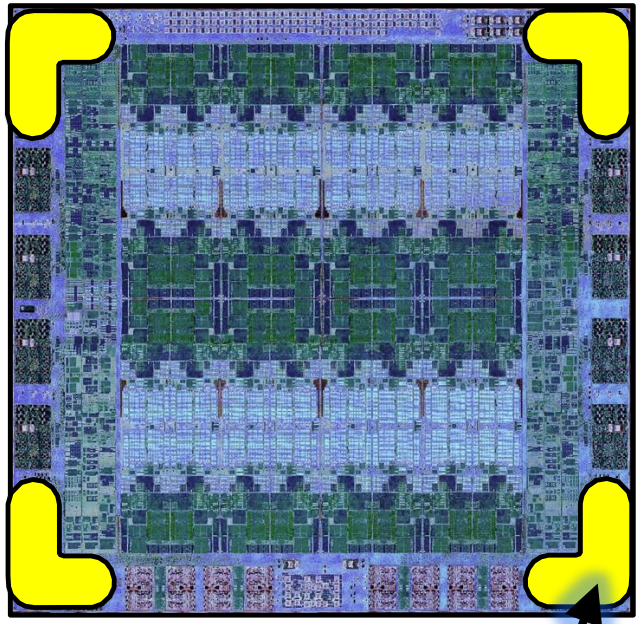
- 1204mm^2 7nm (36B devices)
- Throughput / Socket
  - Up to 30 SMT8 Cores (3.5+ GHz)
- Compute & I/O Density
  - Memory: x128 @ 32 GT/s
  - SMP/Cluster/Accel: x192 @ 32 GT/s
  - I/O: x64 PCIe G5
  - 1 to 4 sockets

Up to 4 DCM Sockets



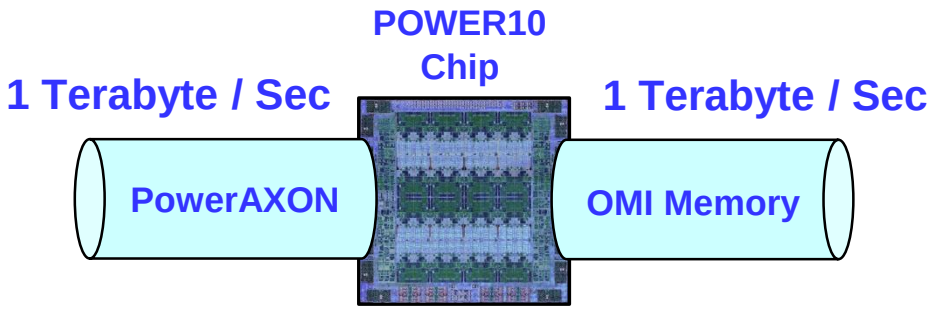
(Multi-socket configurations show processor capability only, and do not imply system product offerings)

System Composability: PowerAXON & Open Memory Interfaces

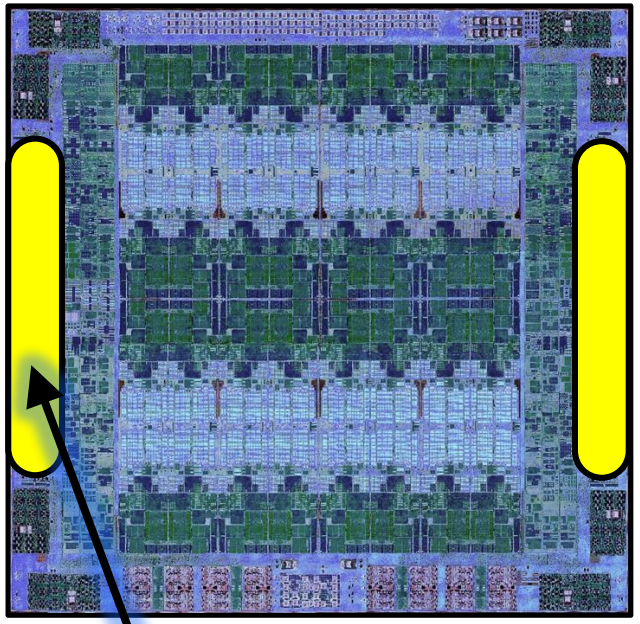


PowerAXON corner
4x8 @ 32 GT/s

Multi-protocol
“Swiss-army-knife”
Flexible / Modular Interfaces



Built on best-of-breed
Low Power, Low Latency,
High Bandwidth
Signaling Technology



OMI edge
8x8 @ 32 GT/s

6x bandwidth / mm^2
compared to DDR4
signaling

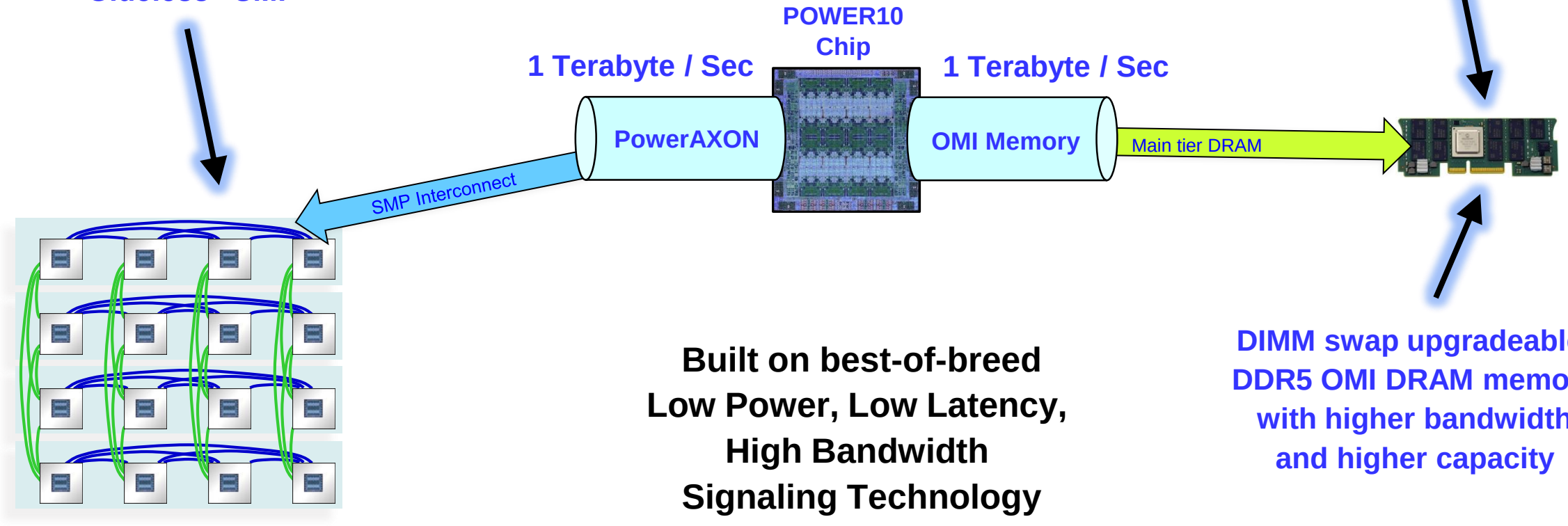
System Enterprise Scale and Bandwidth: SMP & Main Memory

Multi-protocol
“Swiss-army-knife”
Flexible / Modular Interfaces

Allocate the bandwidth
however you need to use it

Initial Offering:
Up to 4 TB / socket
OMI DRAM memory
410 GB/s peak bandwidth
(MicroChip DDR4 buffer)
< 10ns latency adder

Build up to 16 SCM socket
Robustly Scalable
High Bisection Bandwidth
“Glueless” SMP



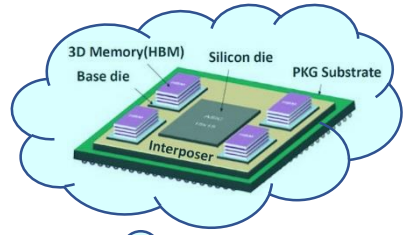
Built on best-of-breed
Low Power, Low Latency,
High Bandwidth
Signaling Technology

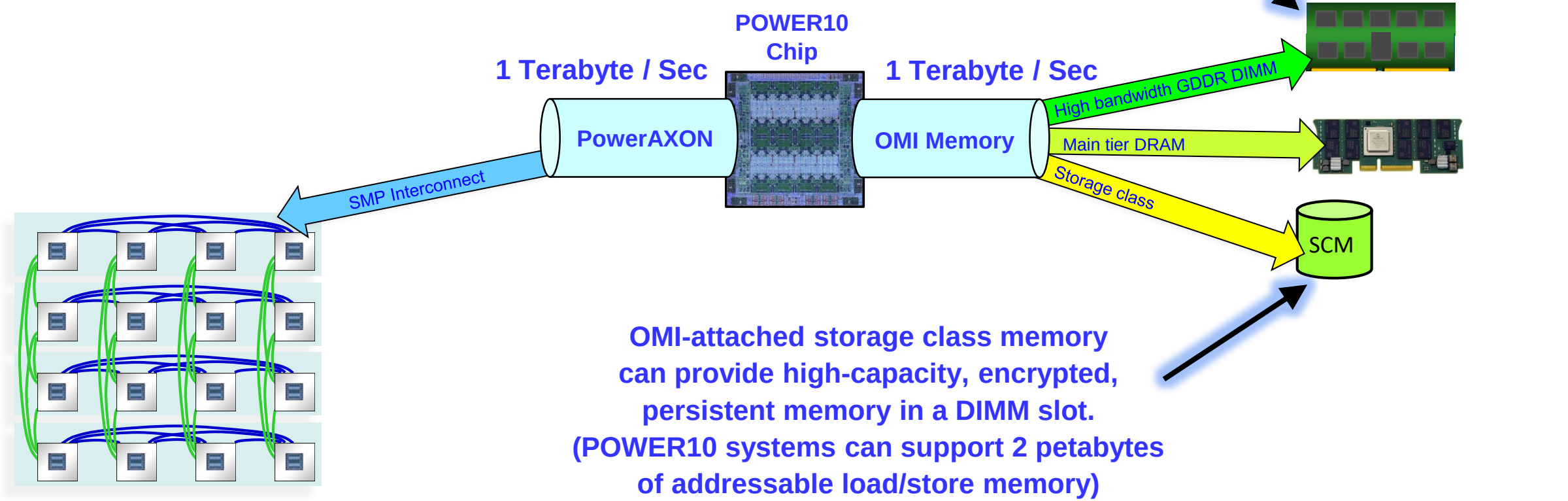
DIMM swap upgradeable:
DDR5 OMI DRAM memory
with higher bandwidth
and higher capacity

(PowerAXON and OMI Memory configurations show processor capability only, and do not imply system product offerings)

Data Plane Bandwidth and Capacity: Open Memory Interfaces

OMI-attached GDDR DIMMs can provide low-capacity, high bandwidth alternative to HBM, without packaging rigidity & cost (Up to 800 GB/s sustained)



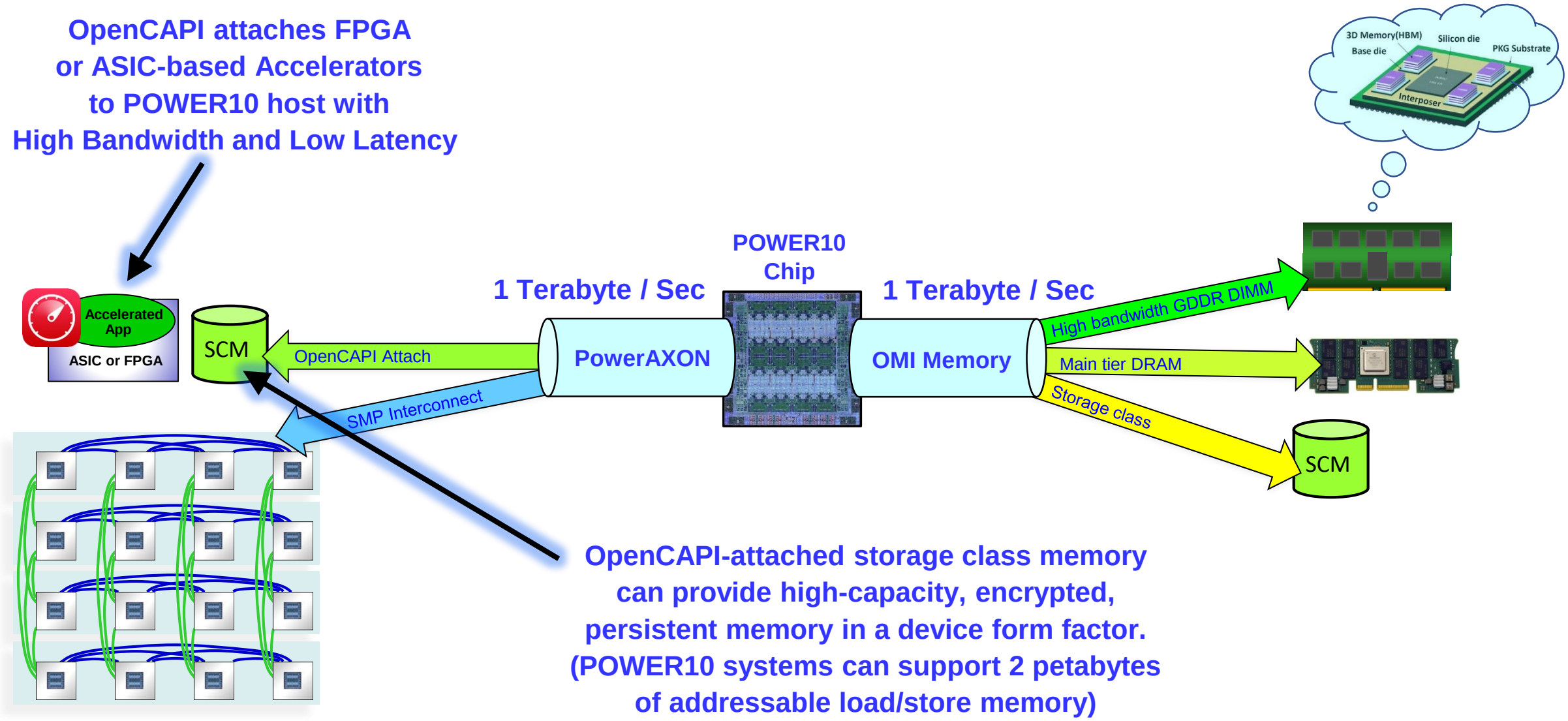


OMI-attached storage class memory can provide high-capacity, encrypted, persistent memory in a DIMM slot. (POWER10 systems can support 2 petabytes of addressable load/store memory)

(PowerAXON and OMI Memory configurations show processor capability only, and do not imply system product offerings)

System Heterogeneity and Data Plane Capacity: OpenCAPI

OpenCAPI attaches FPGA or ASIC-based Accelerators to POWER10 host with High Bandwidth and Low Latency

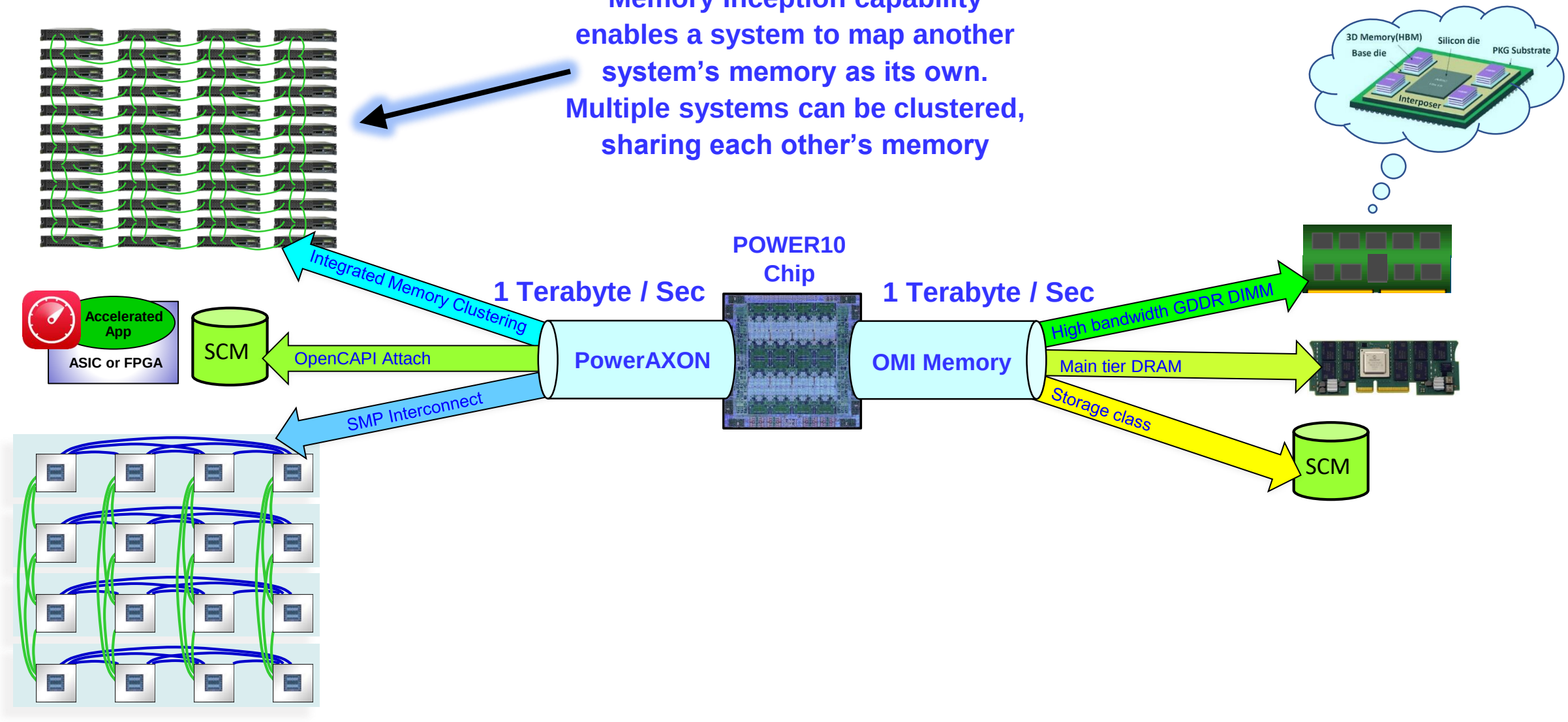


OpenCAPI-attached storage class memory can provide high-capacity, encrypted, persistent memory in a device form factor. (POWER10 systems can support 2 petabytes of addressable load/store memory)

(PowerAXON and OMI Memory configurations show processor capability only, and do not imply system product offerings)

Pod Composability: PowerAXON Memory Clustering

Memory Inception capability enables a system to map another system's memory as its own. Multiple systems can be clustered, sharing each other's memory



(PowerAXON and OMI Memory configurations show processor capability only, and do not imply system product offerings)

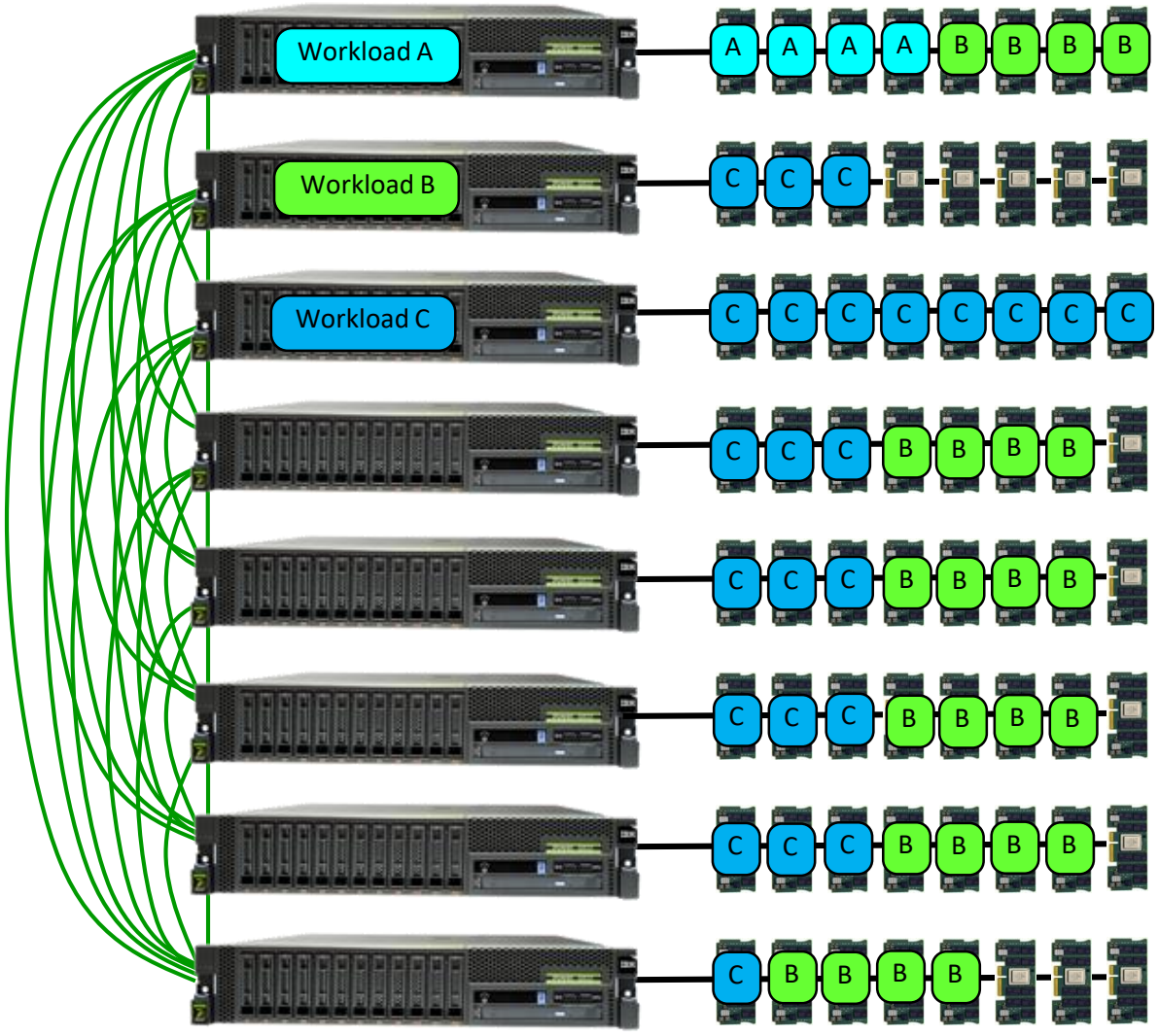
Memory Clustering: Distributed Memory Disaggregation and Sharing

Use case: Share load/store memory amongst directly connected neighbors within Pod
Unlike other schemes, memory can be used:
- As low latency local memory
- As NUMA latency remote memory

Example: Pod = 8 systems each with 8TB
Workload A Rqmt: 4 TB low latency
Workload B Rqmt: 24 TB relaxed latency
Workload C Rqmt: 8 TB low latency plus 16TB relaxed latency

All Rqmts met by configuration shown

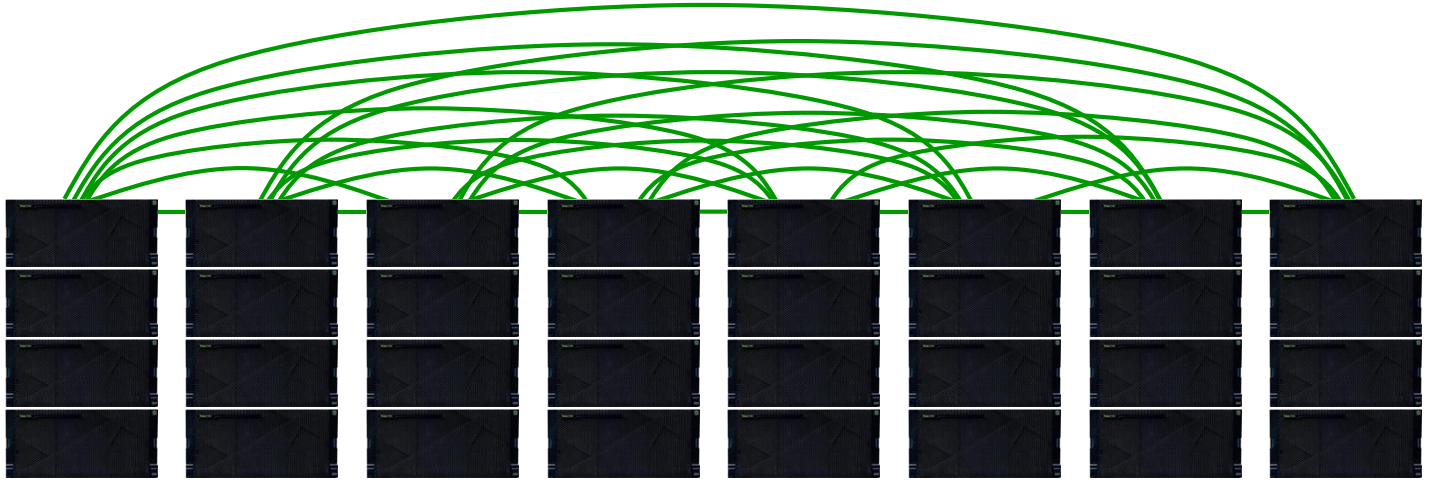
POWER10 2 Petabyte memory size enables much larger configurations



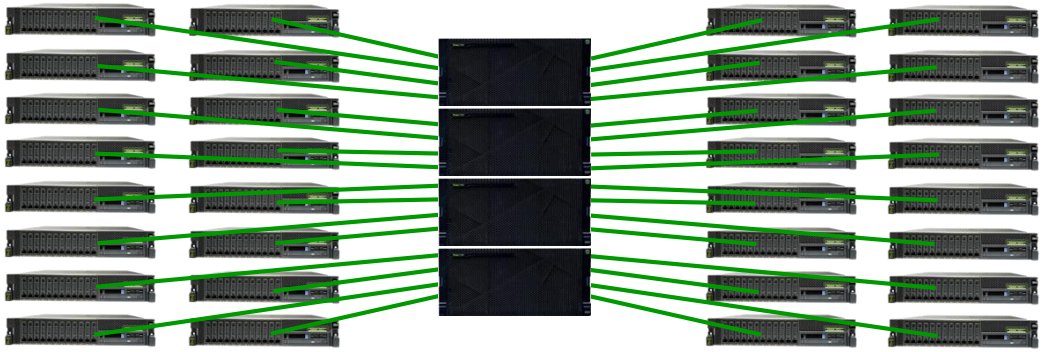
(Memory cluster configurations show processor capability only, and do not imply system product offerings)

Memory Clustering: Enterprise-Scale Memory Sharing

Pod of Large Enterprise Systems
Distributed Sharing at Petabyte Scale



Or Hub-and-spoke with memory server and memory-less compute nodes

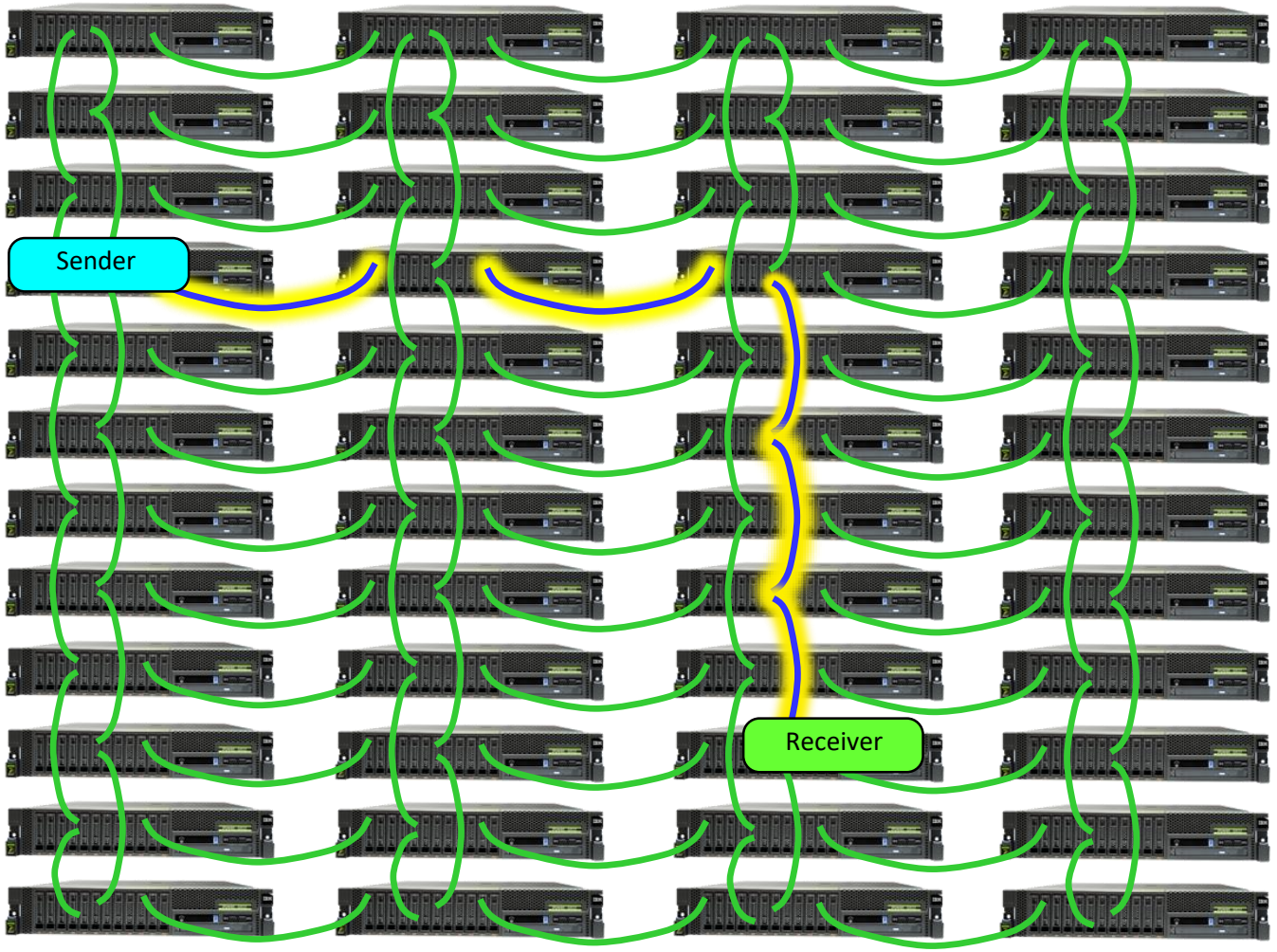


(Memory cluster configurations show processor capability only, and do not imply system product offerings)

Memory Clustering: Pod-level Clustering

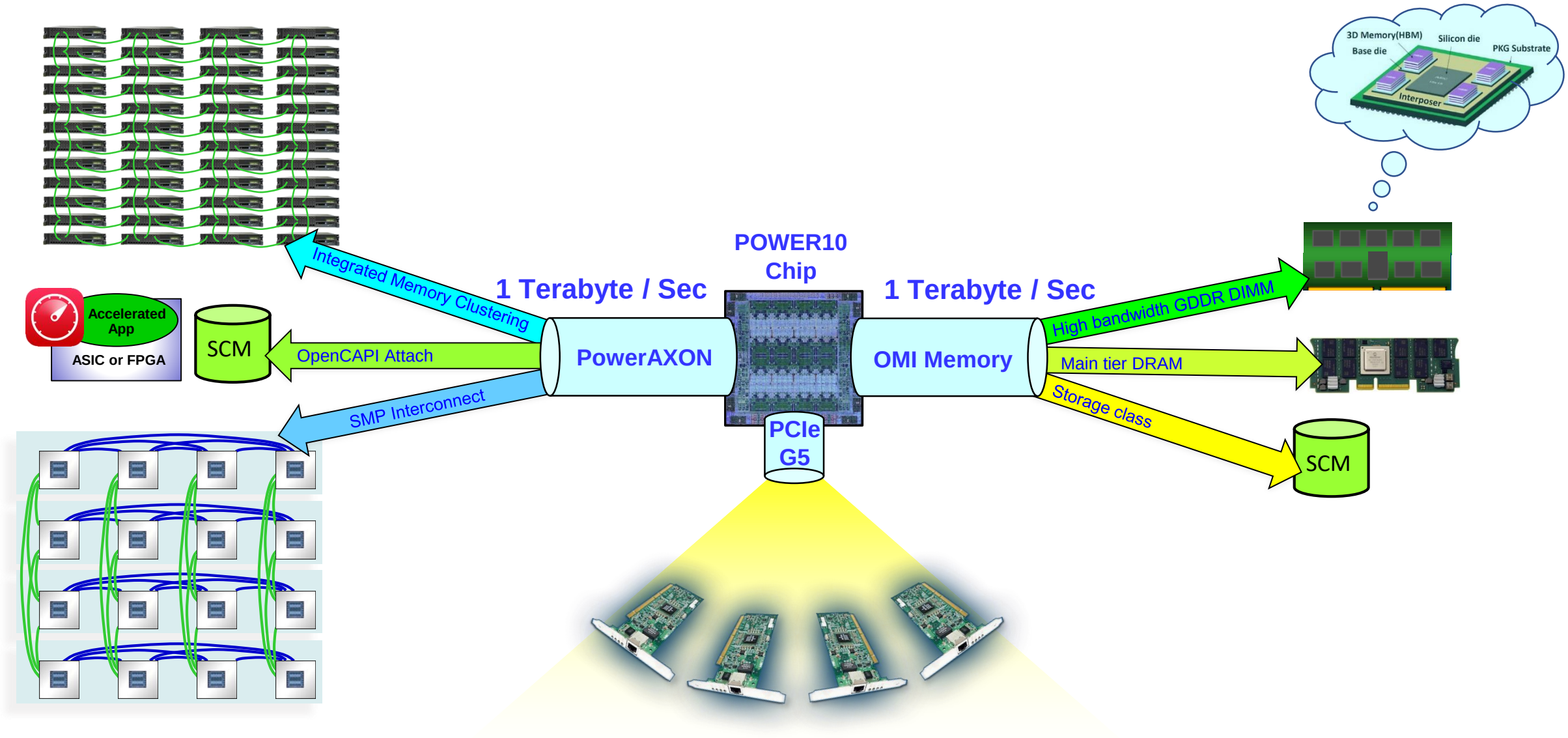
Use case: Low latency, high bandwidth messaging scaling to 1000's of nodes

Leverage 2 Petabyte addressability to create memory window into each destination for messaging mailboxes



(Memory cluster configurations show processor capability only, and do not imply system product offerings)

System Composability: PCIe Gen 5 Industry I/O Attach



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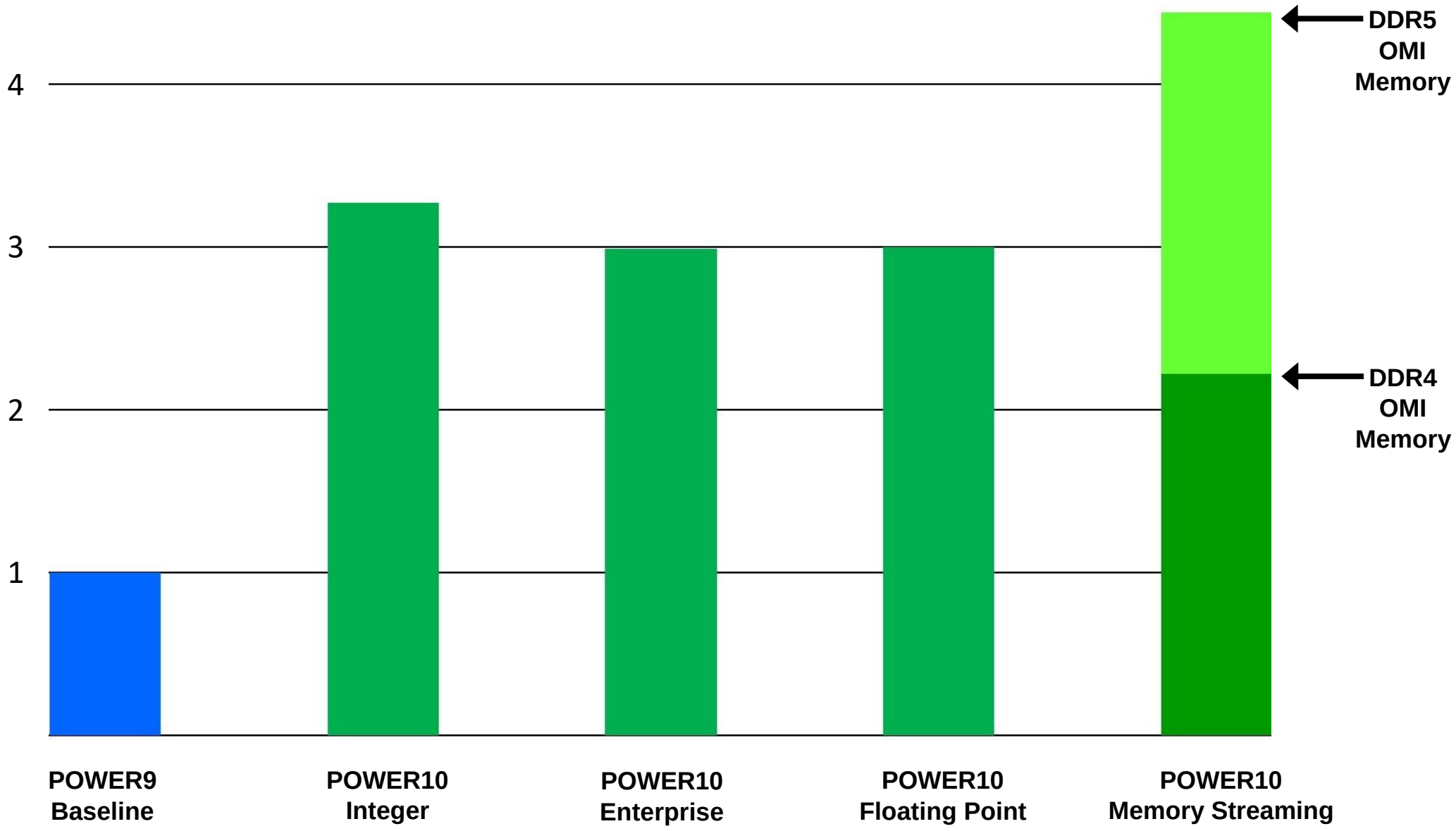
POWER10 General Purpose Socket Performance Gains



(Performance assessments based upon pre-silicon engineering analysis of POWER10 dual-socket server offering vs POWER9 dual-socket server offering)

Powerful Core = Enterprise Strength + AI Infused

New Enterprise Micro-architecture

- Flexibility
  - Up to 8 threads per core / 240 per socket
- Optimized for performance and efficiency
  - +30% avg. core performance*
  - +20% avg. single thread performance*
  - 2.6x core performance efficiency* (3x @ socket)

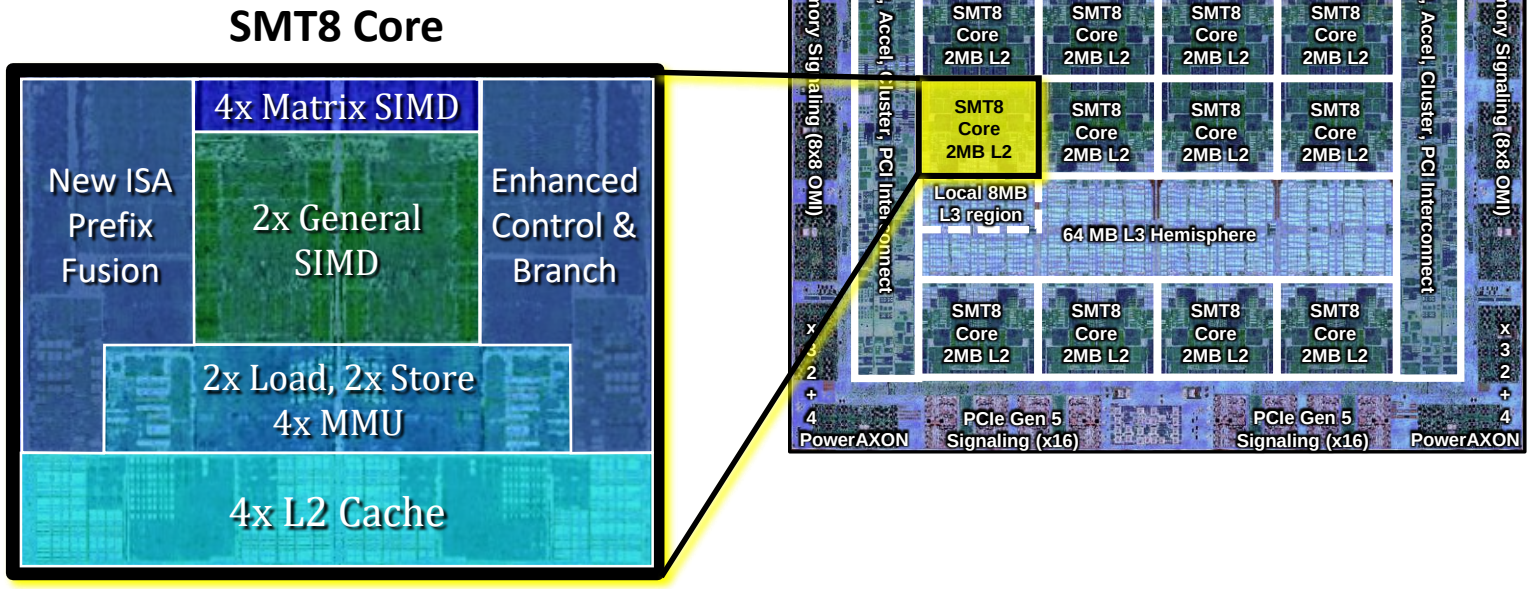
AI Infused

- 4x matrix SIMD acceleration*
- 2x bandwidth & general SIMD*
- 4x L2 cache capacity with improved thread isolation*
- New ISA with AI data-types

* versus POWER9

1-2 POWER10 chips per socket

- Up to **30 SMT8 Cores**
- Up to **60 SMT4 Cores**



(Performance assessments based upon pre-silicon engineering analysis of POWER10 dual-socket server offering vs POWER9 dual-socket server offering)

Powerful Core : Enterprise Flexibility

Multiple World-class Software Stacks

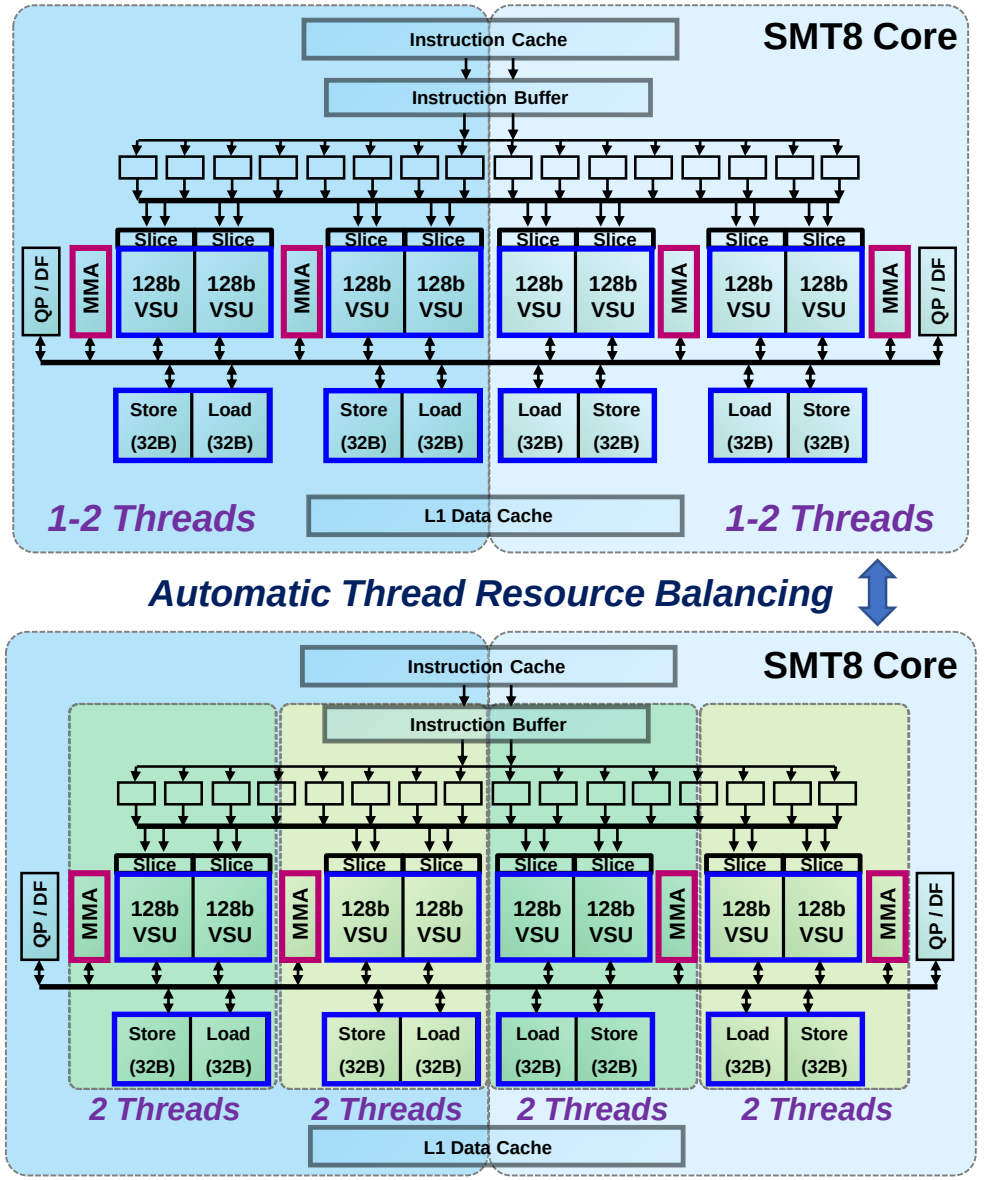
Resilience and full stack integrity

- PowerVM, KVM
- AIX, IBMi, Linux on Power, OpenShift

Partition flexibility and security

- Full-core level LPAR
- Thread-based LPAR scheduling
- *NEW*: With PowerVM Hypervisor
  - Nested KVM + PowerVM
  - Hardware assisted container/VM isolation

Hardware Based Workload Balance



IBM POWER10

Powerful Architecture : AI Infused and Future Ready

POWER10 implements Power ISA v3.1

- v3.1 was the latest open Power ISA contributed to the OpenPOWER Foundation: Royalty free and inclusive of patents for compliant designs

OpenPOWER™

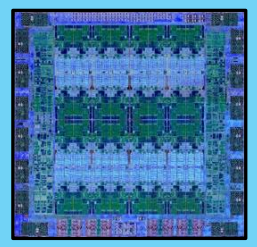
POWER10 Architecture – Feature Highlights		
Prefix Architecture	Greatly expanded opcode space, pc-relative addressing, MMA masking, etc.	RISC friendly 8B instructions including modified and new opcode forms. 
New Instructions and Datatypes	New Scalar instructions for control flow, and operation symmetry	Set Boolean extensions; quad-precision extensions; 128b integer extensions; test LSB by byte; byte reverse GPR; int mul/div modulo; string isolate/clear; pause, wait-reserve.
	New SIMD instructions for AI, throughput and data manipulation	32-byte load/store vector-pair; MMA (matrix math assist) with reduced precision; bfloat-16 converts; permute variations: extract, insert, splat, blend; compress/expand assist; mask generation; bit manipulation.
Advanced System Features and Ease of Use	Storage management	Persistent memory barrier / flush; store sync; translation extensions.
	Debug	PMU sampling, filtering; debug watchpoints; tracing.
	Hot/Cold page tracking	Recording for memory management.
	Copy/Paste extensions	Memory movement; continued on-chip acceleration: Gzip, 842 compression, AES/SHA.
Advanced EnergyScale	Adaptive power management	Additional performance boost across the operating range.
Security for Cloud	Transparent isolation and security for enterprise cloud workloads	Nested virtualization with KVM on PowerVM; secure containers; main memory encryption; dynamic execution control; secure PMU.

Security : End-to-End for the Enterprise Cloud

Cloud Workload Security

Secure Virtualization

Processor Security Foundations



Application Security

VM's
Applications
Services

VM's
Applications
Middleware

Container Container Container Container Container Container

AIX for Business Linux OPENSHIFT

Confidential Computing

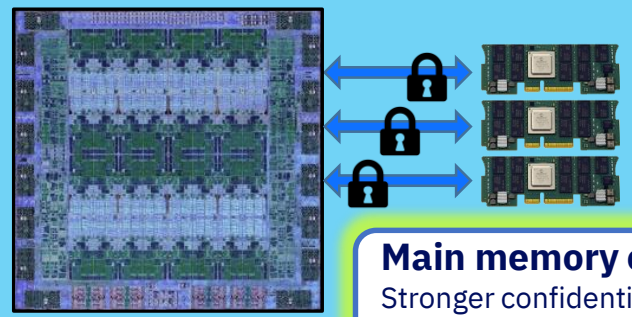
Secure Containers:
- Transparent to applications
- End-to-end encryption

PowerVM KVM PowerVM

Nested Virtualization – KVM on PowerVM:
- Stronger container isolation without performance penalty
- HW enabled and transparent

Crypto Performance:
- Core crypto improvements for today's algorithms (AES, SHA3) and ready for the future (PQC, FHE)

Dynamic Execution Control Register (DEXCR)



Hardened container memory isolation

Main memory encryption:
Stronger confidentiality against physical attacks

Performance enhanced side channel avoidance

IBM POWER10

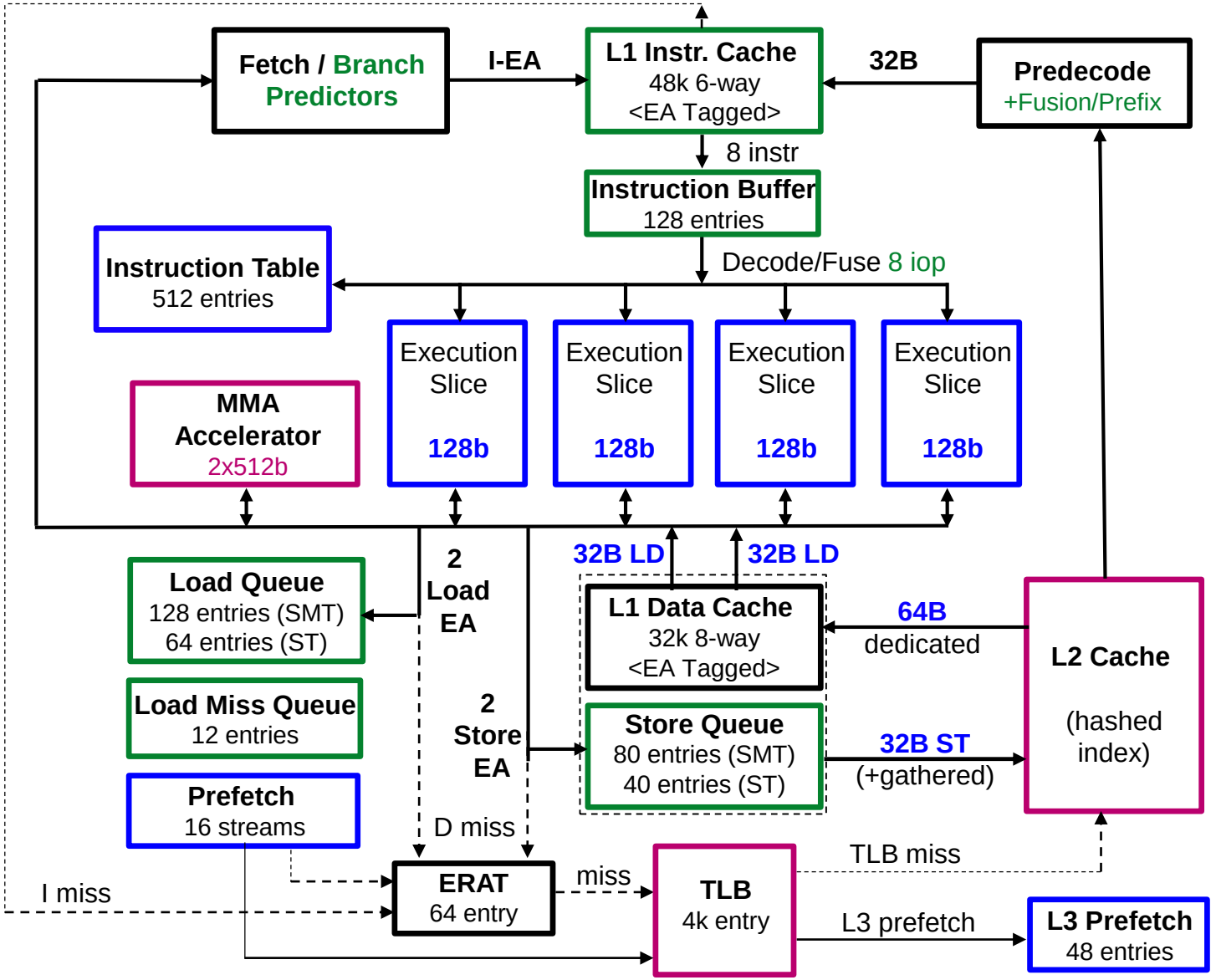
Powerful Core : Enterprise Strength

PERFORMANCE

WATT

P10 Core Micro-architecture

½ SMT8 Core Resources Shown = SMT4 Core Equivalent



Capacity vs. POWER9: ***Improved*** | ***>= 2x*** | ***= 4x***

IBM POWER10

Powerful Core : Enterprise Strength

PERFORMANCE

- **Double SIMD + Inference acceleration**
  - 2x SIMD, 4x MMA, 4x AES/SHA

WATT

P10 Core Micro-architecture

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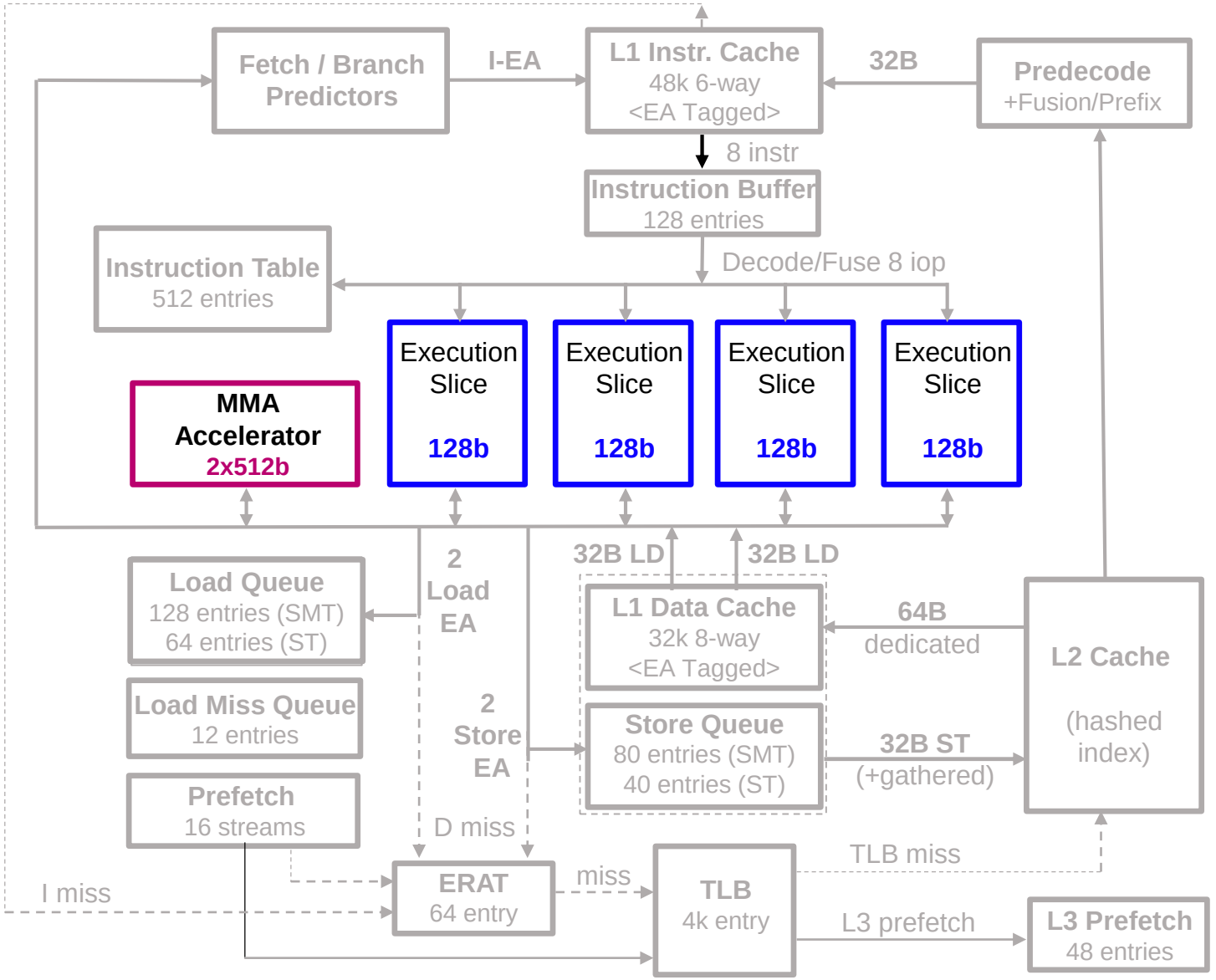

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- **Larger working-sets**
  - 1.5x L1-Instruction cache, 4x L2, 4x TLB

WATT

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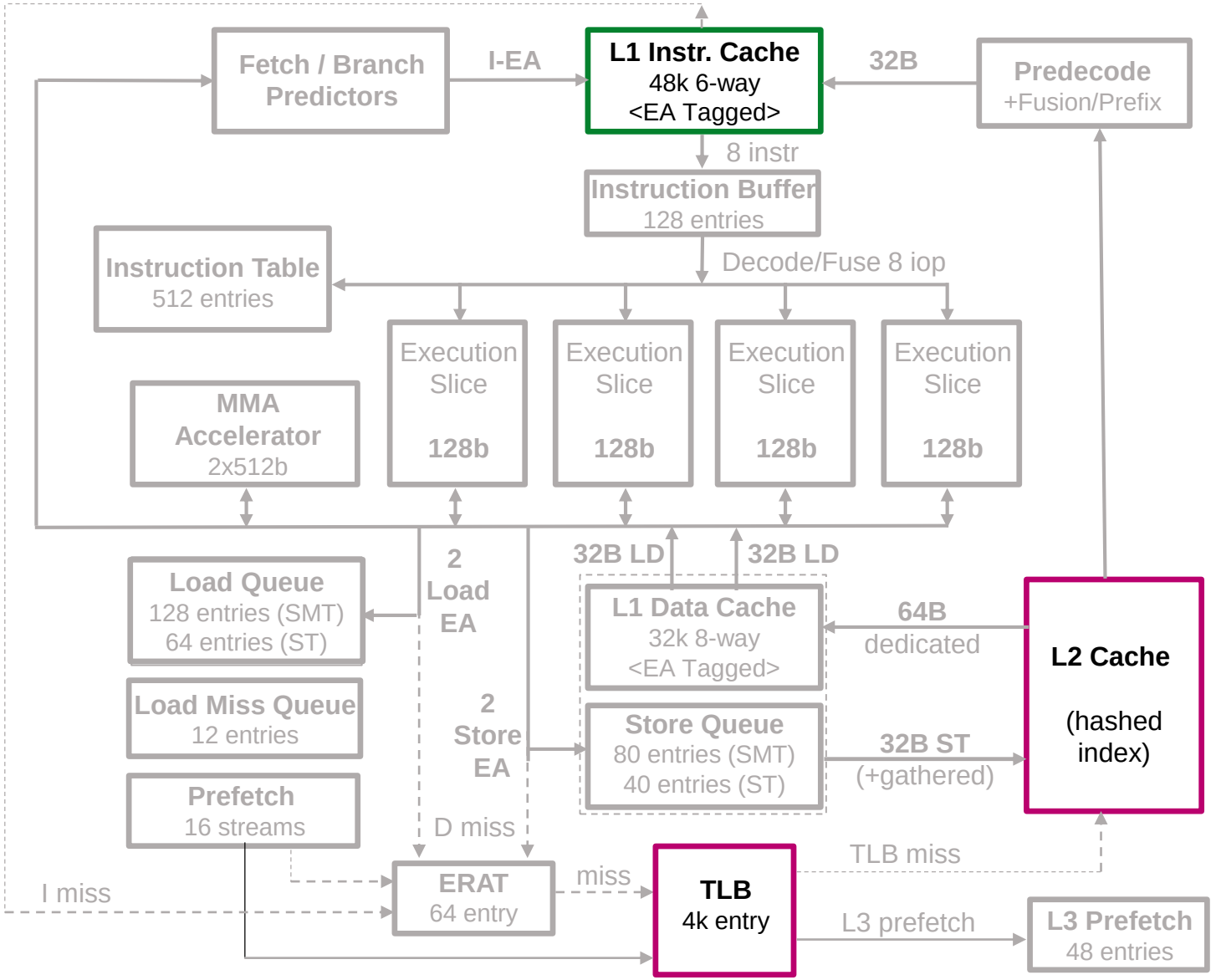

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WATT

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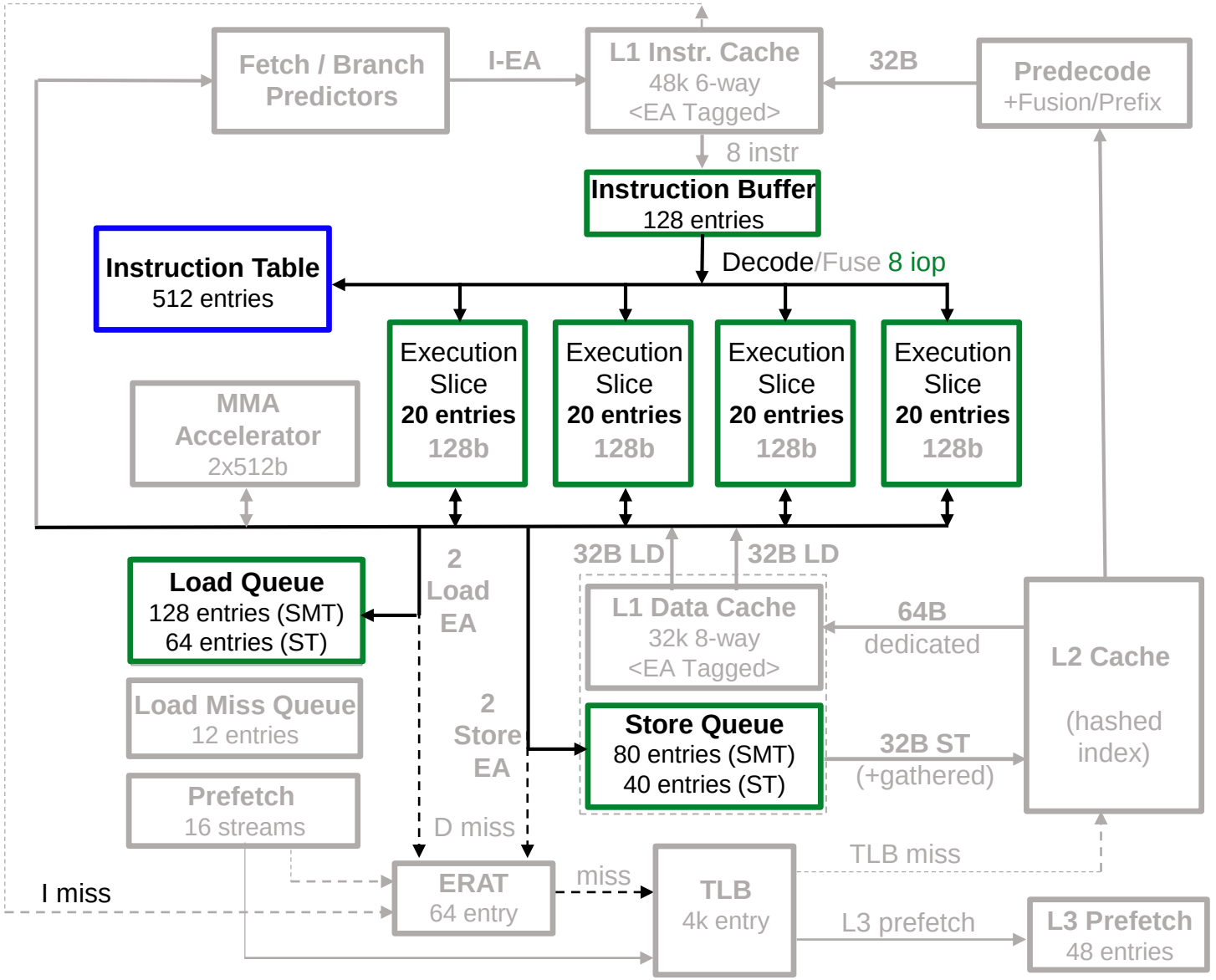

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- **Deeper/wider instruction windows**
- **Data latency (cycles)**
  - L2 13.5 (minus 2), L3 27.5 (minus 8)
  - L1-D cache 4 +0 for Store forward (minus 2)
  - TLB access +8.5 (minus 7)

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P10 Core Micro-architecture

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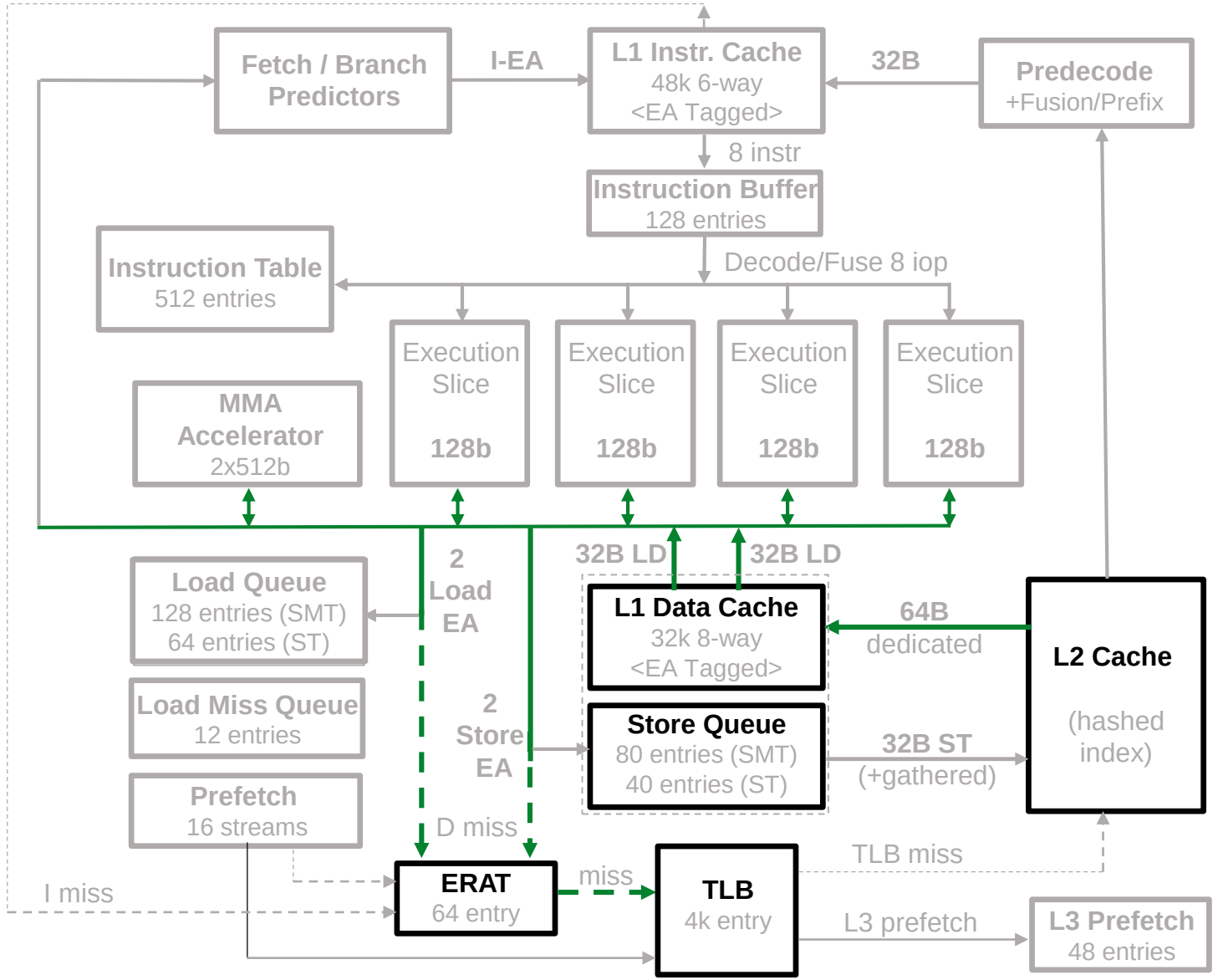

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IBM POWER10

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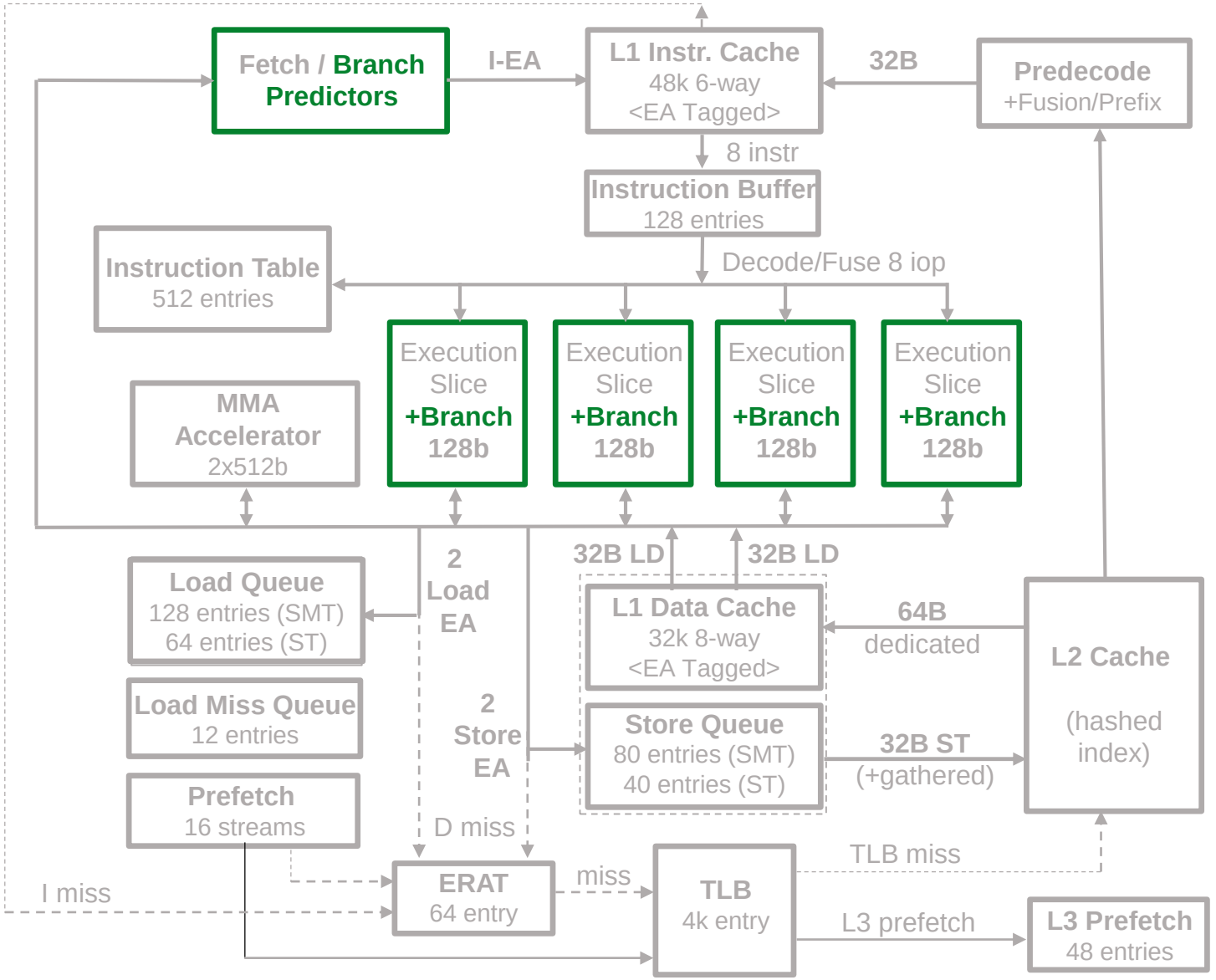
- **Branch**
  - Target registers with GPR in main regfile
  - New predictors: target and direction, 2x BHT

WATT

P10 Core Micro-architecture

½ SMT8 Core Resources Shown = SMT4 Core Equivalent



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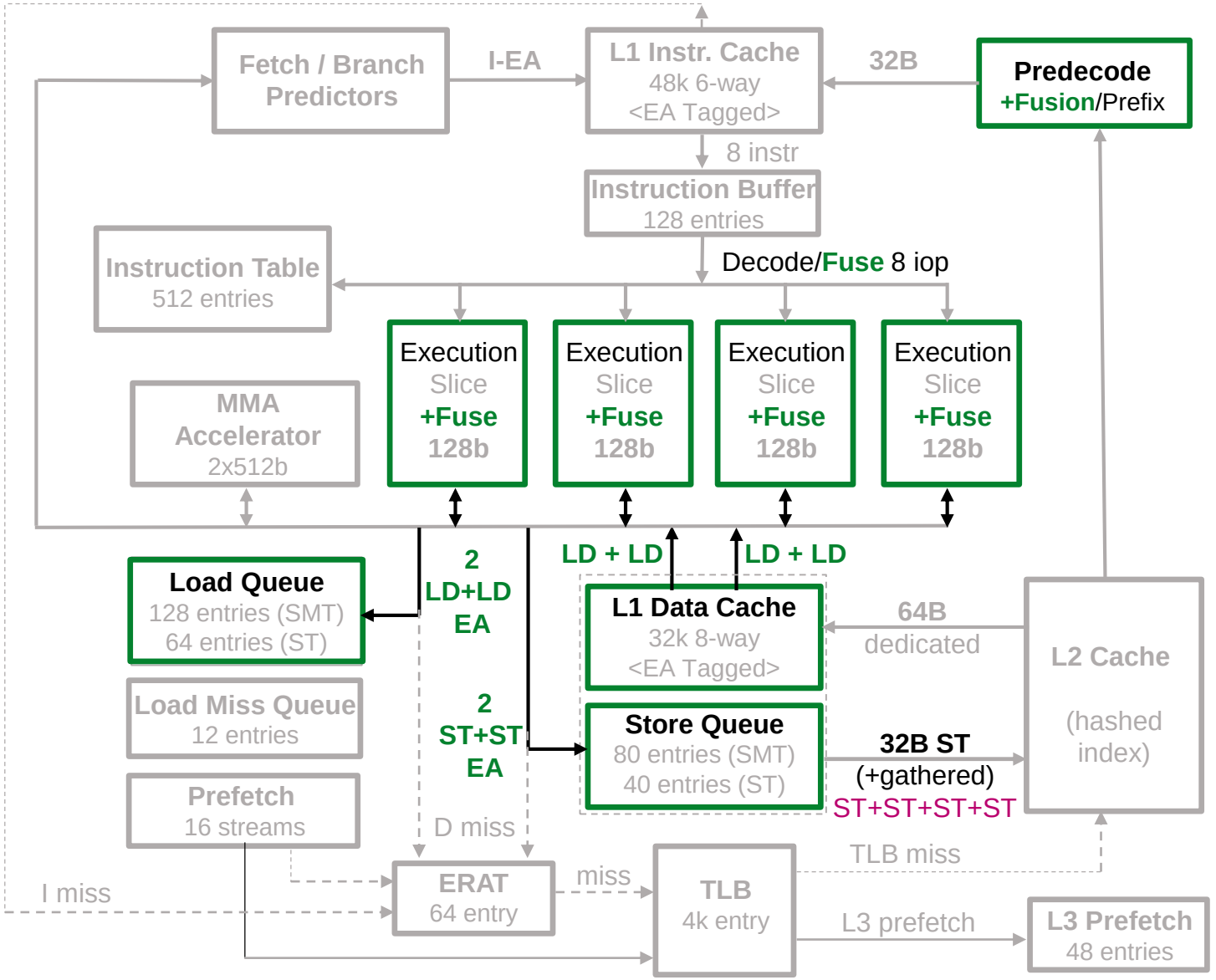
- **Branch**
  - Target registers with GPR in main regfile
  - New predictors: target and direction, 2x BHT
- **Fusion**
  - Fixed, SIMD, other: merge and back to back
  - Load, store : consecutive storage

WATT

P10 Core Micro-architecture

½ SMT8 Core Resources Shown = SMT4 Core Equivalent



Capacity vs. POWER9: *Improved* | *>= 2x* | *= 4x*

IBM POWER10

Powerful Core : Energy Efficient

PERFORMANCE

- **Double SIMD + Inference acceleration**
  - 2x SIMD, 4x MMA, 4x AES/SHA
- **Larger working-sets**
  - 1.5x L1-Instruction cache, 4x L2, 4x TLB
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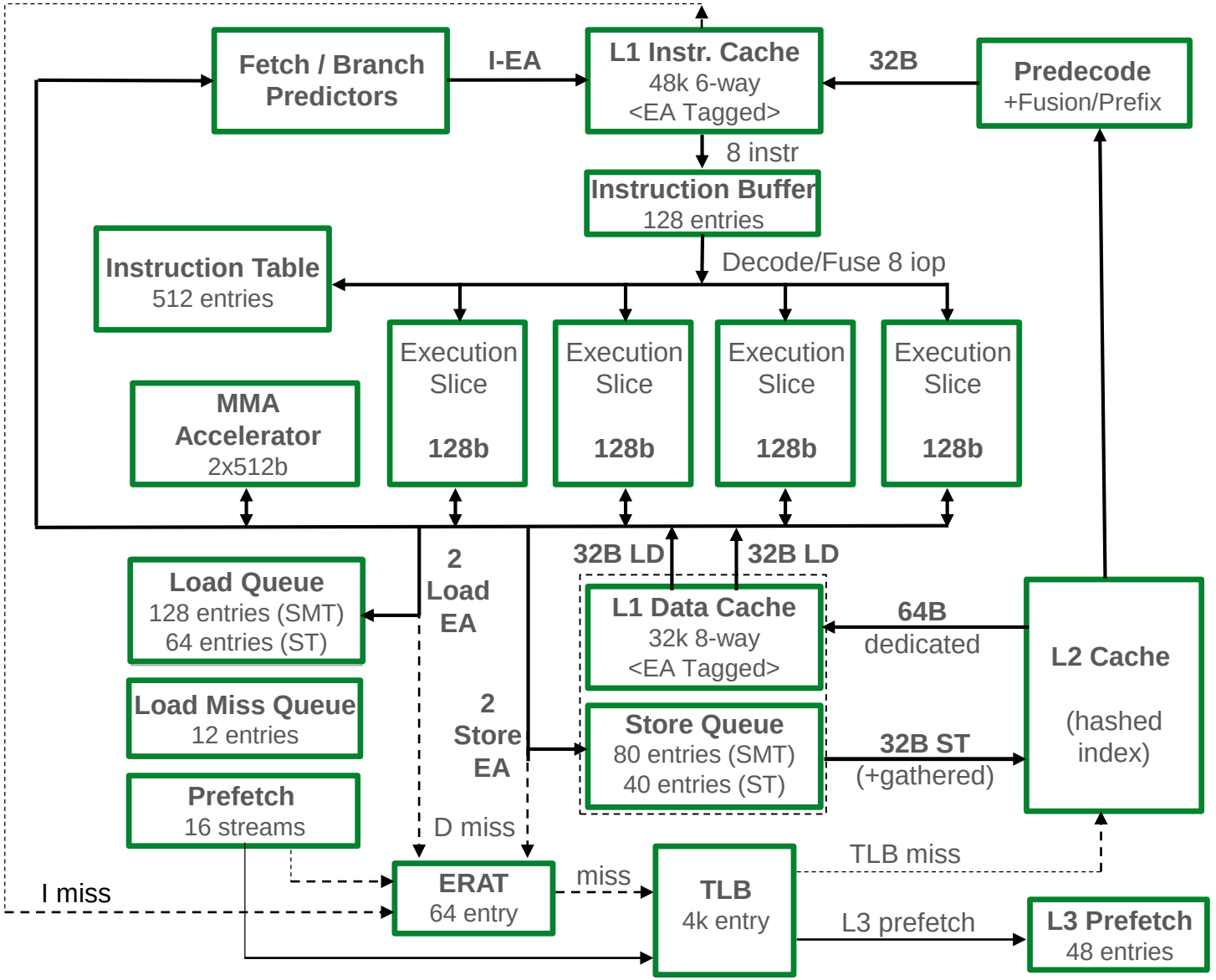
WATT

- **Improved clock-gating**
- **Design & micro-arch efficiency**

P10 Core Micro-architecture

½ SMT8 Core Resources Shown = SMT4 Core Equivalent



Watt vs. POWER9: ***Improved***

IBM POWER10

Powerful Core : Energy Efficient

PERFORMANCE

- **Double SIMD + Inference acceleration**
  - 2x SIMD, 4x MMA, 4x AES/SHA
- **Larger working-sets**
  - 1.5x L1-Instruction cache, 4x L2, 4x TLB
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P10 Core Micro-architecture

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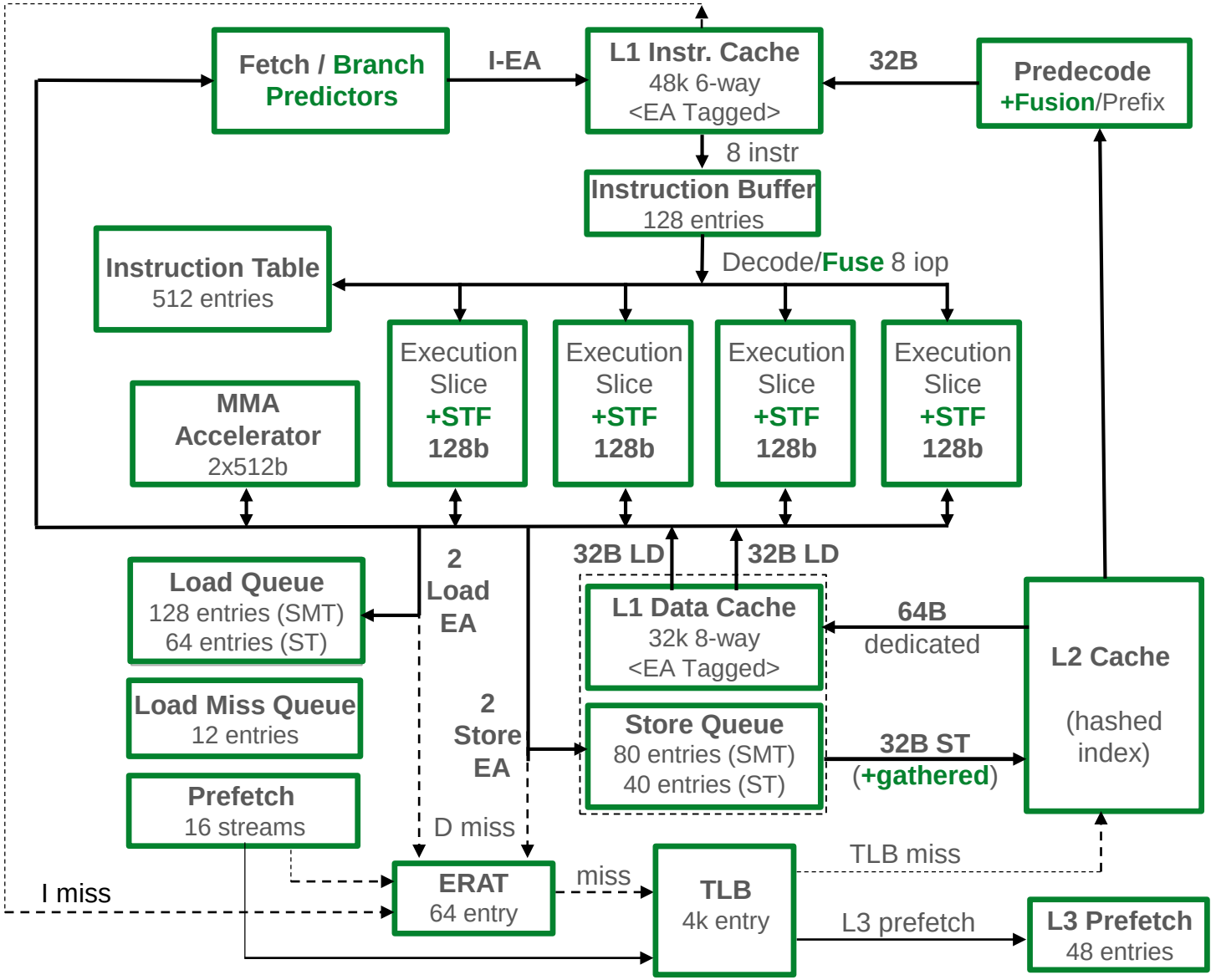

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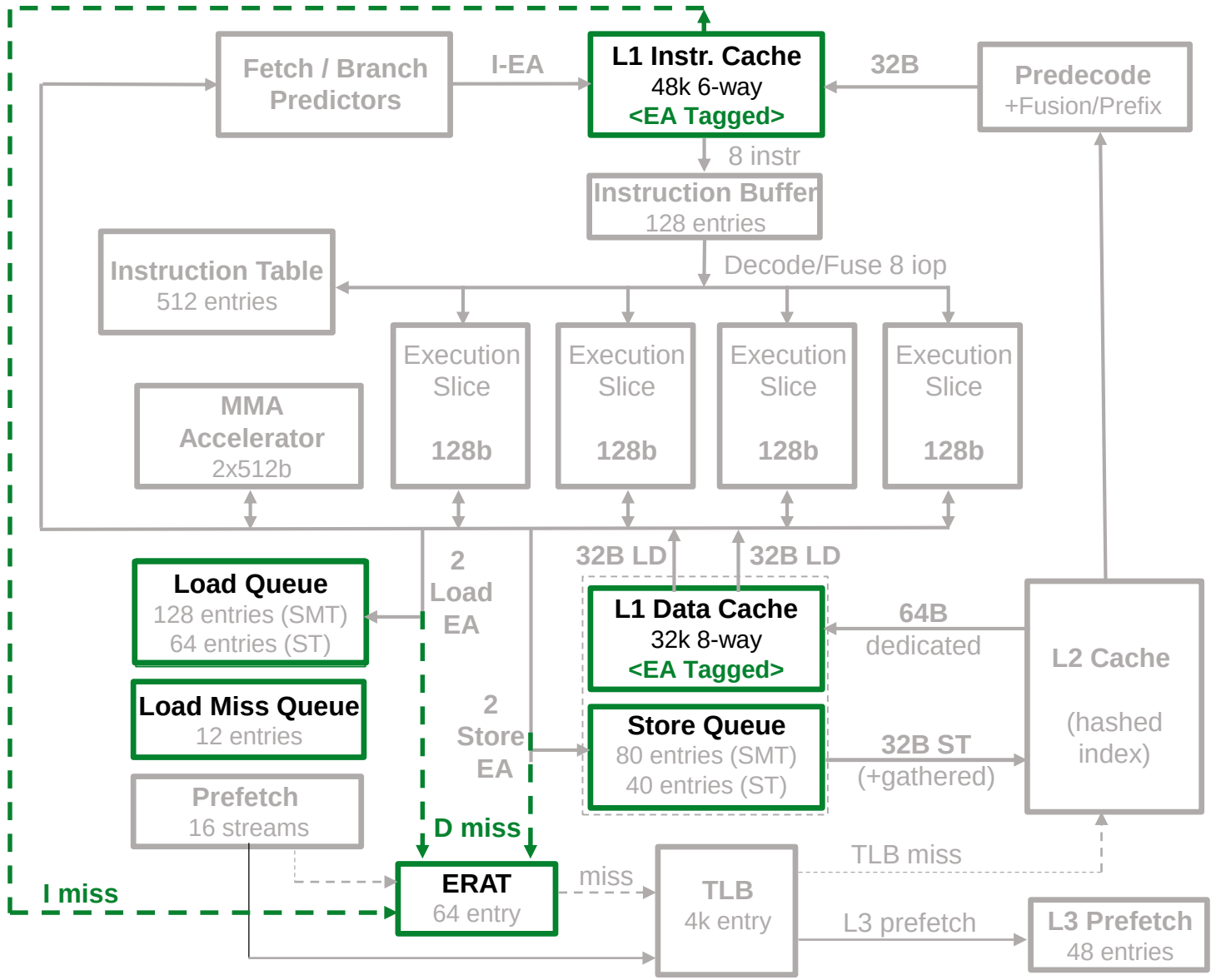

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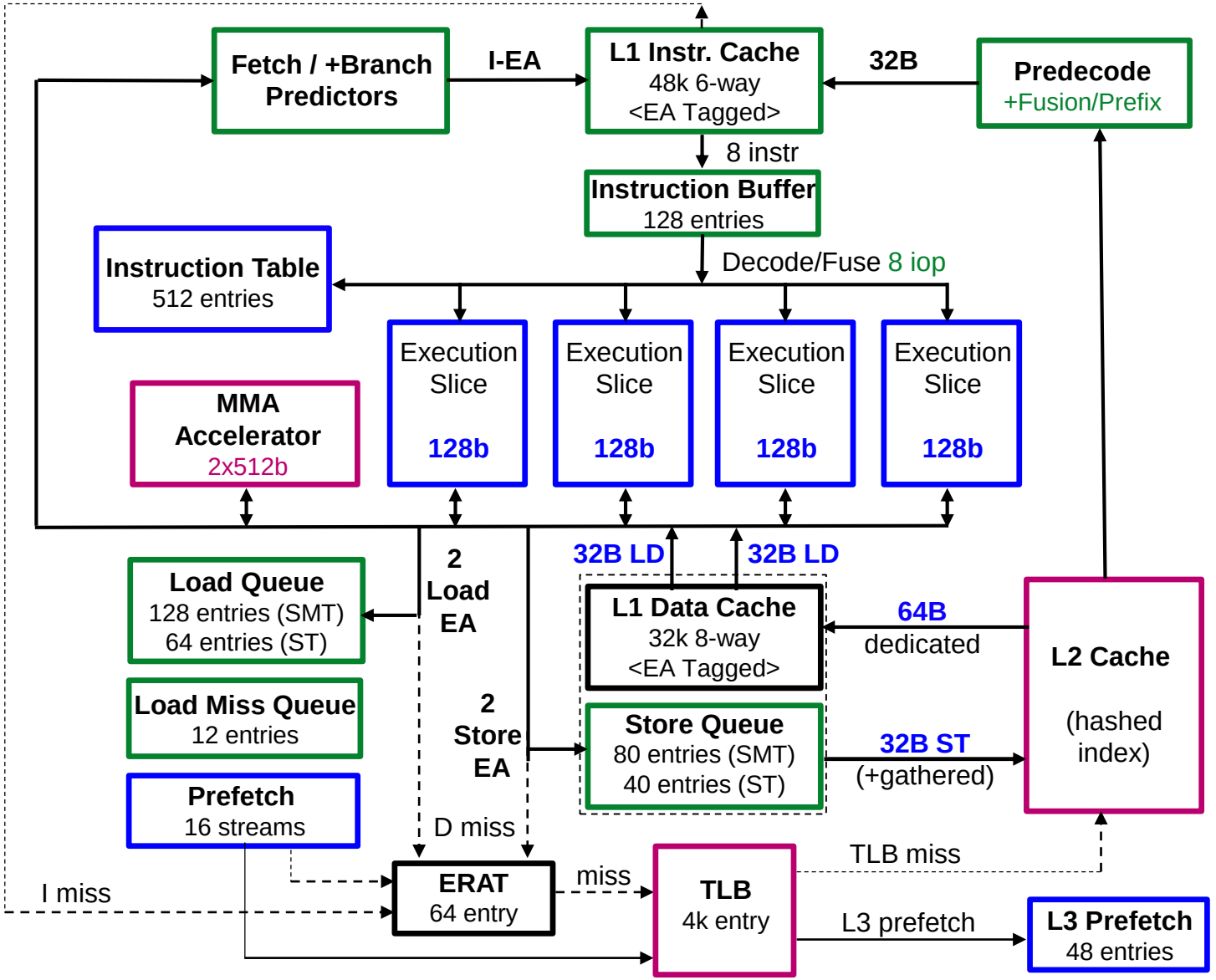

Capacity vs. POWER9: *Improved* | *>= 2x* | *= 4x*

IBM POWER10

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$$\frac{1.3x}{0.5x} = 2.6x$$ **performance / watt**

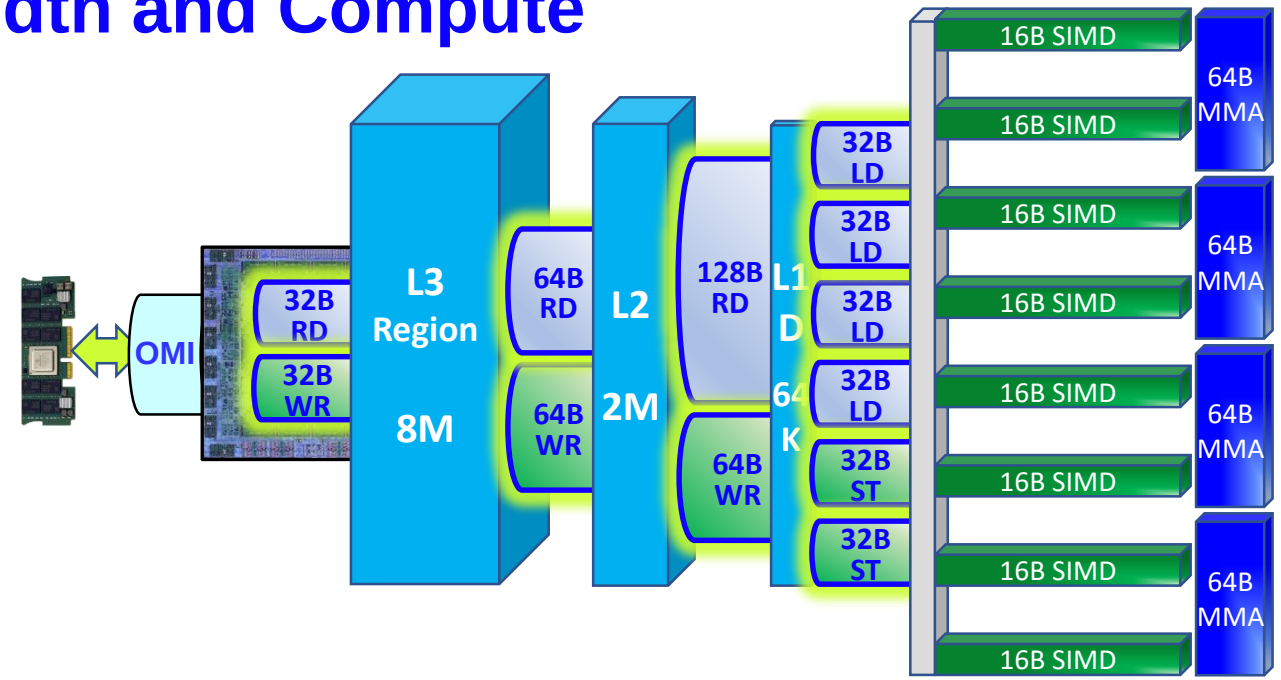
POWER10 vs. POWER9 Core

Powerful Core : AI Infused Bandwidth and Compute

BYTES / FLOP

2x Bytes from all sources

(OMI, L3, L2, L1 caches*)



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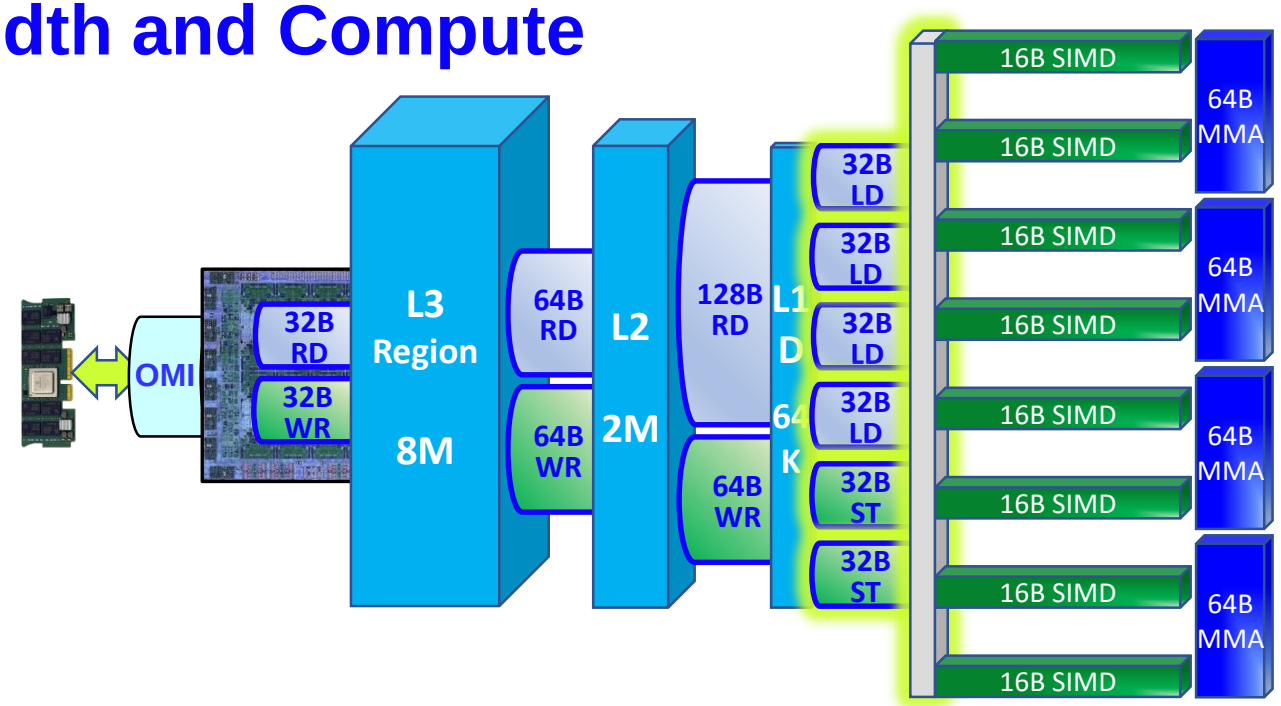

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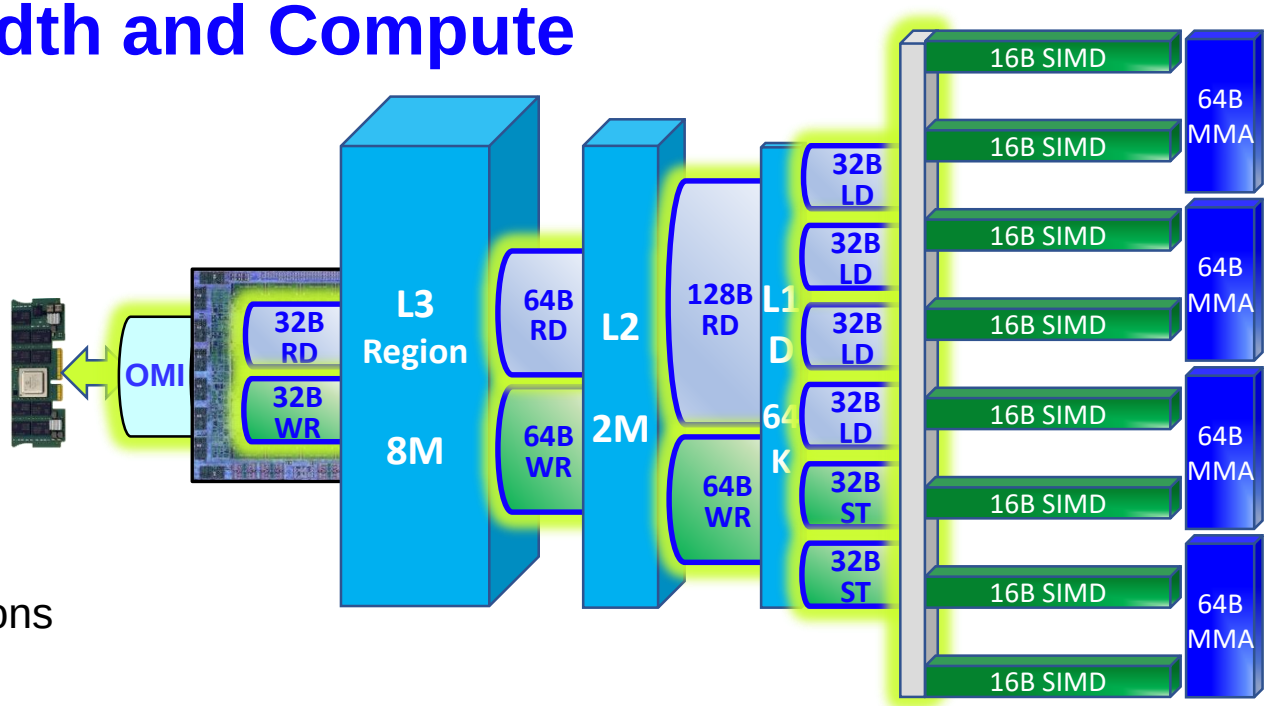

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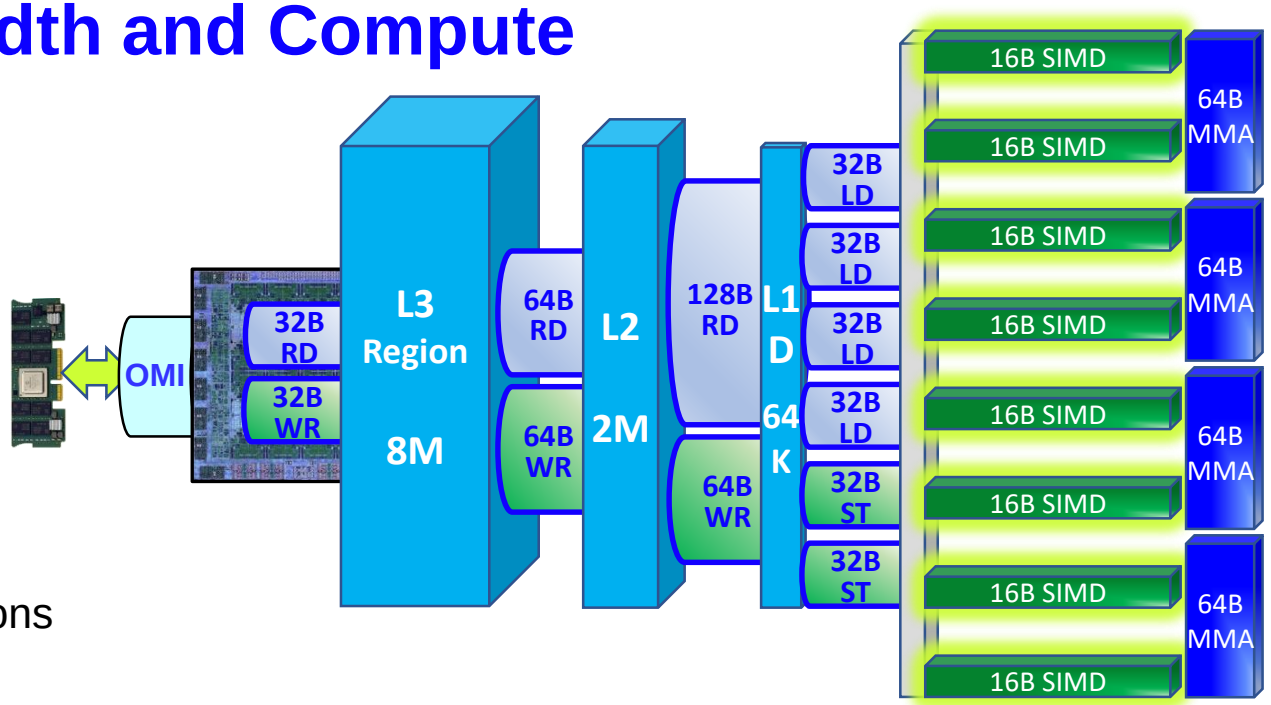

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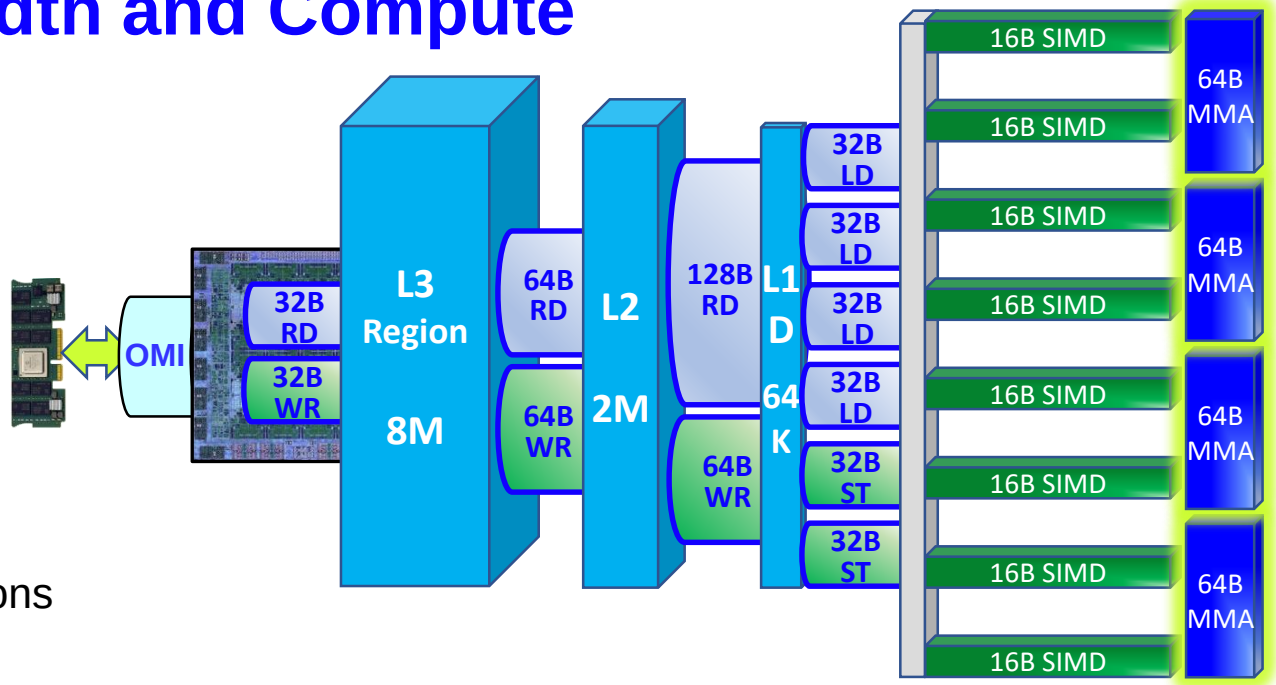

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4-32x Matrix Math Acceleration*

- **4 512b engines per core = 2048b results / cycle**
  - Matrix math outer products: $A \leftarrow \{\pm\}A\ \{\pm\}\ XY^T$
  - Double, Single, Reduced precision

Rank	Operand Type (X,Y)			*Accumulator*	Peak [FL]OPS / cycle		
k	Type	X	Y^T	A	Instruction	Thread	SMT8 Core
1	Float-64 DP	4×1	1×2	4×2 (Fp-64)	16	32	64
	Float-32 SP	4×1	1×4	4×4 (Fp-32)	32	64	128
2	Float-16 HP	4×2	2×4		64	128	256
	Bfloat-16 HP	4×2	2×4				
	Int-16	4×2	2×4	4×4 (Int-32)			
4	Int-8	4×4	4×4		128	256	512
8	Int 4	4×8	8×4		256	512	1024

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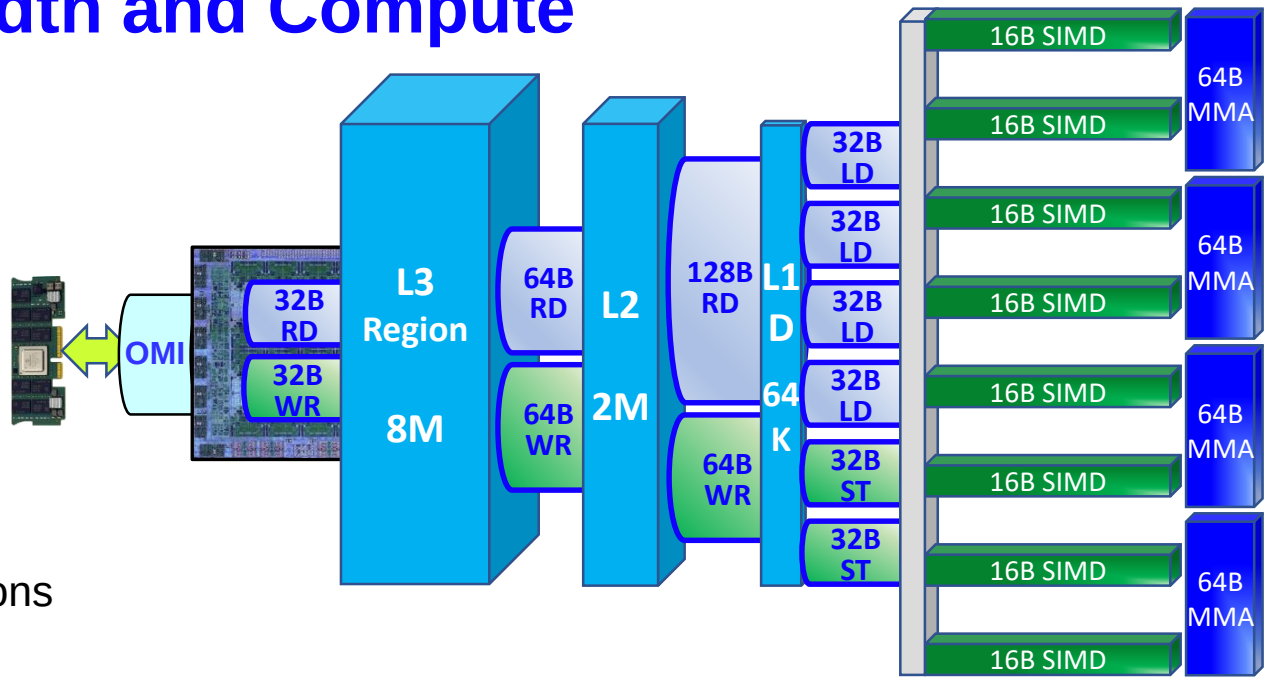

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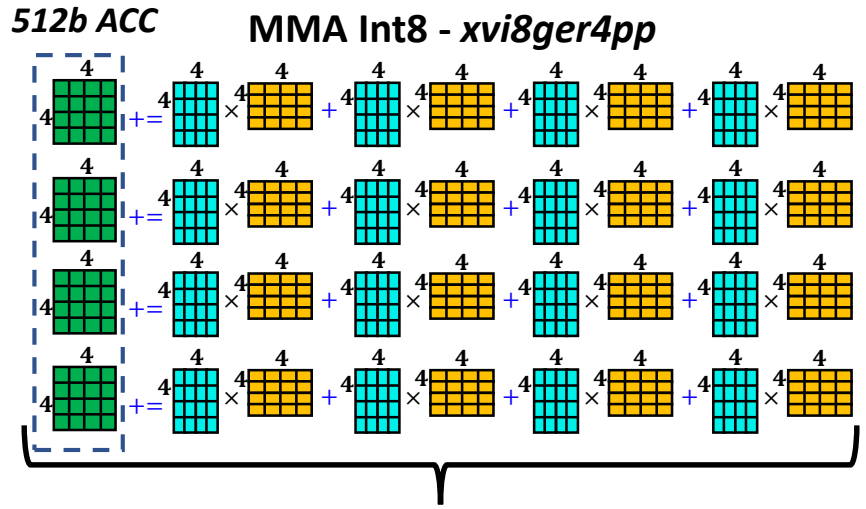
* versus POWER9

AI Infused Core: Inference Acceleration

- **4x+ per core throughput**
- **3x → 6x thread latency reduction (SP, int8)***

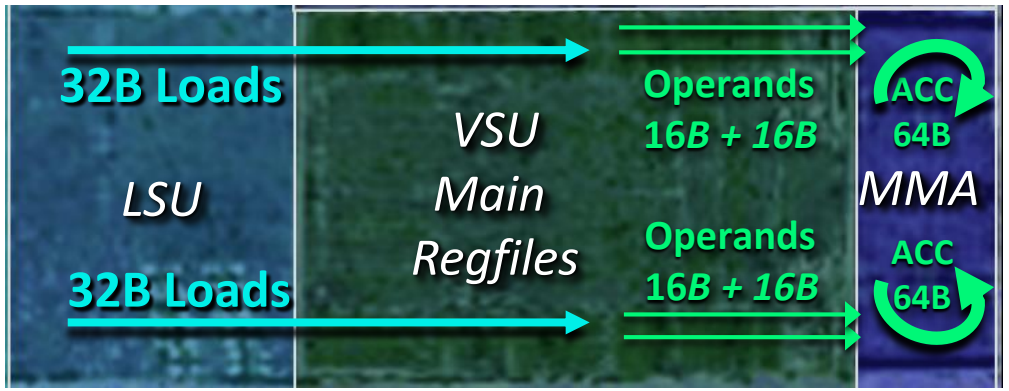
- **POWER10 Matrix Math Assist (MMA) instructions**
  - 8 512b architected Accumulator (ACC) Registers
  - 4 parallel units per SMT8 core
- **Consistent VSR 128b register architecture**
  - Minimal SW ecosystem disruption – no new register state
  - Application performance via updated library (OpenBLAS, etc.)
  - POWER10 aliases 512b ACC to 4 128b VSR's
    - Architecture allows redefinition of ACC
- **Dense-Math-Engine microarchitecture**
  - Built for data re-use algorithms
  - Includes separate physical register file (ACC)
  - 2x efficiency vs. traditional SIMD for MMA



4 per cycle per SMT8 core

Matrix Optimized / High Efficiency

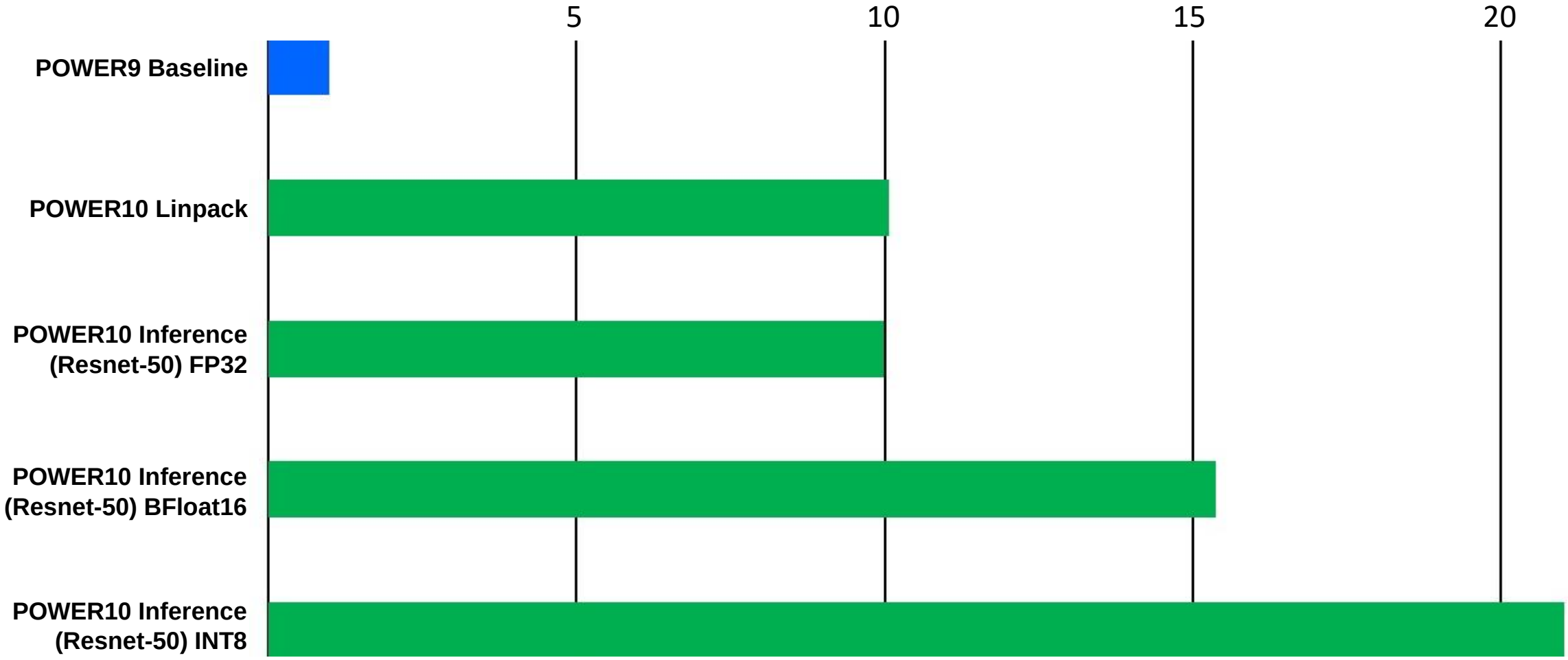
Result data remains local to compute



Inference Accelerator dataflow *(2 per SMT8 core)*

* versus POWER9

POWER10 SIMD / AI Socket Performance Gains



(Performance assessments based upon pre-silicon engineering analysis of POWER10 dual-socket server offering vs POWER9 dual-socket server offering)