POWER10 Processor Chip

**Technology and Packaging:**
- 602mm² 7nm Samsung (18B devices)
- 18 layer metal stack, enhanced device
- Single-chip or Dual-chip sockets

**Computational Capabilities:**
- Up to 15 SMT8 Cores (2 MB L2 Cache / core)
  (Up to 120 simultaneous hardware threads)
- Up to 120 MB L3 cache (low latency NUCA mgmt)
- 3x energy efficiency relative to POWER9
- Enterprise thread strength optimizations
- AI and security focused ISA additions
- 2x general, 4x matrix SIMD relative to POWER9
- EA-tagged L1 cache, 4x MMU relative to POWER9

**Open Memory Interface:**
- 16 x8 at up to 32 GT/s (1 TB/s)
- Technology agnostic support: near/main/storage tiers
- Minimal (< 10ns latency) add vs DDR direct attach

**PowerAXON Interface:**
- 16 x8 at up to 32 GT/s (1 TB/s)
- SMP interconnect for up to 16 sockets
- OpenCAPI attach for memory, accelerators, I/O
- Integrated clustering (memory semantics)

**PCle Gen 5 Interface:**
- x64 / DCM at up to 32 GT/s
Socket Composability: **SCM & DCM**

**Single-Chip Module Focus:**
- 602mm$^2$ 7nm (18B devices)
- Core/thread Strength
  - Up to 15 SMT8 Cores (4+ GHz)
- Capacity & Bandwidth / Compute
  - Memory: x128 @ 32 GT/s
  - SMP/Cluster/Accel: x128 @ 32 GT/s
  - I/O: x32 PCIe G5
- System Scale (Broad Range)
  - 1 to 16 sockets

**Dual-Chip Module Focus:**
- 1204mm$^2$ 7nm (36B devices)
- Throughput / Socket
  - Up to 30 SMT8 Cores (3.5+ GHz)
- Compute & I/O Density
  - Memory: x128 @ 32 GT/s
  - SMP/Cluster/Accel: x192 @ 32 GT/s
  - I/O: x64 PCIe G5
  - 1 to 4 sockets

(Multi-socket configurations show processor capability only, and do not imply system product offerings)
System Composability: **PowerAXON & Open Memory Interfaces**

Multi-protocol
“Swiss-army-knife”
Flexible / Modular Interfaces

Built on best-of-breed
Low Power, Low Latency,
High Bandwidth
Signaling Technology

**PowerAXON corner**
4x8 @ 32 GT/s

**OMI Memory**
8x8 @ 32 GT/s

6x bandwidth / mm²
compared to DDR4 signaling
System Enterprise Scale and Bandwidth: **SMP & Main Memory**

- **Multi-protocol**
  - "Swiss-army-knife"
  - Flexible / Modular Interfaces

- **Build up to 16 SCM socket**
  - Robustly Scalable
  - High Bisection Bandwidth
  - "Glueless" SMP

- **1 Terabyte / Sec**
  - POWERAXON
  - OMI Memory

- **Allocate the bandwidth however you need to use it**

- **Built on best-of-breed**
  - Low Power, Low Latency,
  - High Bandwidth
  - Signaling Technology

- **Initial Offering:**
  - Up to 4 TB / socket
  - OMI DRAM memory
  - 410 GB/s peak bandwidth
  - (MicroChip DDR4 buffer)
  - < 10ns latency adder

- **DIMM swap upgradeable:**
  - DDR5 OMI DRAM memory
  - with higher bandwidth
  - and higher capacity

(PowerAXON and OMI Memory configurations show processor capability only, and do not imply system product offerings)
Data Plane Bandwidth and Capacity: **Open Memory Interfaces**

OMI-attached GDDR DIMMs can provide low-capacity, high bandwidth alternative to HBM, without packaging rigidity & cost (Up to 800 GB/s sustained)

OMI-attached storage class memory can provide high-capacity, encrypted, persistent memory in a DIMM slot. (POWER10 systems can support 2 petabytes of addressable load/store memory)

(PowerAXON and OMI Memory configurations show processor capability only, and do not imply system product offerings)
OpenCAPI attaches FPGA or ASIC-based Accelerators to POWER10 host with High Bandwidth and Low Latency.

OpenCAPI-attached storage class memory can provide high-capacity, encrypted, persistent memory in a device form factor. (POWER10 systems can support 2 petabytes of addressable load/store memory)

(PowerAXON and OMI Memory configurations show processor capability only, and do not imply system product offerings)
Pod Composability: PowerAXON Memory Clustering

Memory Inception capability enables a system to map another system’s memory as its own. Multiple systems can be clustered, sharing each other’s memory.

(PowerAXON and OMI Memory configurations show processor capability only, and do not imply system product offerings)
Use case: Share load/store memory amongst directly connected neighbors within Pod
Unlike other schemes, memory can be used:
- As low latency local memory
- As NUMA latency remote memory

Example: Pod = 8 systems each with 8TB
Workload A Rqmt: 4 TB low latency
Workload B Rqmt: 24 TB relaxed latency
Workload C Rqmt: 8 TB low latency plus 16TB relaxed latency

All Rqmts met by configuration shown

POWER10 2 Petabyte memory size enables much larger configurations

(Memory cluster configurations show processor capability only, and do not imply system product offerings)
Memory Clustering: Enterprise-Scale Memory Sharing

Pod of Large Enterprise Systems
Distributed Sharing at Petabyte Scale

Or Hub-and-spoke with memory server
and memory-less compute nodes

(Memory cluster configurations show processor capability only, and do not imply system product offerings)
Memory Clustering: Pod-level Clustering

Use case: Low latency, high bandwidth messaging scaling to 1000’s of nodes

Leverage 2 Petabyte addressability to create memory window into each destination for messaging mailboxes

(Memory cluster configurations show processor capability only, and do not imply system product offerings)
System Composability: PCIe Gen 5 Industry I/O Attach

(PowerAXON and OMI Memory configurations show processor capability only, and do not imply system product offerings)
IBM POWER10

POWER10 General Purpose Socket Performance Gains

(Performance assessments based upon pre-silicon engineering analysis of POWER10 dual-socket server offering vs POWER9 dual-socket server offering)
Powerful Core = Enterprise Strength + AI Infused

New Enterprise Micro-architecture
- Flexibility
  - Up to 8 threads per core / 240 per socket
- Optimized for performance and efficiency
  - +30% avg. core performance*
  - +20% avg. single thread performance*
  - 2.6x core performance efficiency* (3x @ socket)

AI Infused
- 4x matrix SIMD acceleration*
- 2x bandwidth & general SIMD*
- 4x L2 cache capacity with improved thread isolation*
- New ISA with AI data-types

1-2 POWER10 chips per socket
- Up to 30 SMT8 Cores
- Up to 60 SMT4 Cores

* versus POWER9

(Performance assessments based upon pre-silicon engineering analysis of POWER10 dual-socket server offering vs POWER9 dual-socket server offering)
Multiple World-class Software Stacks

Resilience and full stack integrity
- PowerVM, KVM
- AIX, IBMi, Linux on Power, OpenShift

Partition flexibility and security
- Full-core level LPAR
- Thread-based LPAR scheduling
- NEW: With PowerVM Hypervisor
  - Nested KVM + PowerVM
  - Hardware assisted container/VM isolation
POWER10 implements Power ISA v3.1

- v3.1 was the latest open Power ISA contributed to the OpenPOWER Foundation:
  Royalty free and inclusive of patents for compliant designs

<table>
<thead>
<tr>
<th>POWER10 Architecture – Feature Highlights</th>
<th></th>
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<tbody>
<tr>
<td><strong>Prefix Architecture</strong></td>
<td>Greatly expanded opcode space, pc-relative addressing, MMA masking, etc.</td>
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<tr>
<td></td>
<td>RISC friendly 8B instructions including modified and new opcode forms.</td>
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<tr>
<td></td>
<td><img src="image" alt="Prefix-Suffix Diagram" /></td>
</tr>
<tr>
<td><strong>New Instructions and Datatypes</strong></td>
<td>New Scalar instructions for control flow, and operation symmetry</td>
</tr>
<tr>
<td></td>
<td>Set Boolean extensions; quad-precision extensions; 128b integer extensions; test LSB by byte; byte reverse GPR; int mul/div modulo; string isolate/clear; pause, wait-reserve.</td>
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<tr>
<td></td>
<td>New SIMD instructions for AI, throughput and data manipulation</td>
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<tr>
<td></td>
<td>32-byte load/store vector-pair; MMA (matrix math assist) with reduced precision; bfloat-16 converts; permute variations: extract, insert, splat, blend; compress/expand assist; mask generation; bit manipulation.</td>
</tr>
<tr>
<td><strong>Advanced System Features and Ease of Use</strong></td>
<td>Storage management</td>
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<td>Persistent memory barrier / flush; store sync; translation extensions.</td>
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<td>Debug</td>
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<td>PMU sampling, filtering; debug watchpoints; tracing.</td>
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<td>Hot/Cold page tracking</td>
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<td>Recording for memory management.</td>
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<td>Copy/Paste extensions</td>
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<td>Memory movement; continued on-chip acceleration: Gzip, 842 compression, AES/SHA.</td>
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<tr>
<td><strong>Advanced EnergyScale</strong></td>
<td>Adaptive power management</td>
</tr>
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<td>Additional performance boost across the operating range.</td>
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<tr>
<td><strong>Security for Cloud</strong></td>
<td>Transparent isolation and security for enterprise cloud workloads</td>
</tr>
<tr>
<td></td>
<td>Nested virtualization with KVM on PowerVM; secure containers; main memory encryption; dynamic execution control; secure PMU.</td>
</tr>
</tbody>
</table>
Security: End-to-End for the Enterprise Cloud

**Cloud Workload Security**

**Secure Virtualization**

**Processor Security Foundations**

**Application Security**
- VM's
- Applications
- Services
- Middleware

**Crypto Performance:**
- Core crypto improvements for today's algorithms (AES, SHA3) and ready for the future (PQC, FHE)

**Dynamic Execution Control Register** (DEXCR)

**Main memory encryption:**
- Stronger confidentiality against physical attacks

**Performance enhanced side channel avoidance**

**Confidential Computing**
- Transparent to applications
- End-to-end encryption

**Secure Containers:**
- Transparent to applications
- End-to-end encryption

**Nested Virtualization – KVM on PowerVM:**
- Stronger container isolation without performance penalty
- HW enabled and transparent

**Hardened container memory isolation**

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Powerful Core: Enterprise Strength

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Improved

Capacity vs. POWER9: Improved  >= 2x  = 4x
Powerful Core: Enterprise Strength

- Double SIMD + Inference acceleration
  - 2x SIMD, 4x MMA, 4x AES/SHA

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P10 Core Micro-architecture
½ SMT8 Core Resources Shown = SMT4 Core Equivalent

Fetch / Branch Predictors → L1 Instr. Cache
- 48k 6-way
- <EA Tagged>
- 8 instr

Instruction Table
- 512 entries

Instruction Buffer
- 128 entries

Decode/Fuse 8 iop → Predecode + Fusion/Prefix

Load Queue
- 128 entries (SMT)
- 64 entries (ST)

Load Miss Queue
- 12 entries

Prefetch
- 16 streams

L1 Data Cache
- 32k 8-way
- <EA Tagged>

L2 Cache
- (hashed index)

Execution Slice
- 128b

Execution Slice
- 128b

Execution Slice
- 128b

Execution Slice
- 128b

MMA Accelerator
- 2x512b

Store Queue
- 80 entries (SMT)
- 40 entries (ST)

Store Queue
- 80 entries (SMT)
- 40 entries (ST)

L3 Prefetch
- 48 entries

TLB
- 4k entry

L3 Prefetch
- 48 entries

TLB miss

ERAT
- 64 entry

miss

D miss

2 Store EA

2 Load EA

32B LD

32B LD

64B dedicated

32B ST (+gathered)

L2 Cache

Fetch / Branch Predictors

48k 6-way

<EA Tagged>

Decode/Fuse 8 iop

Predecode + Fusion/Prefix

PE

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PER FORM ANCE
Powerful Core: Enterprise Strength

- Double SIMD + Inference acceleration
  - 2x SIMD, 4x MMA, 4x AES/SHA
- Larger working-sets
  - 1.5x L1-Instruction cache, 4x L2, 4x TLB

IBM POWER10

P10 Core Micro-architecture
½ SMT8 Core Resources Shown = SMT4 Core Equivalent

- L1 Instr. Cache: 48k 6-way (EA Tagged)
- L1 Data Cache: 32k 8-way (EA Tagged)
- L2 Cache: (hashed index)
- L3 Prefetch: 48 entries

- Load Queue: 128 entries (SMT), 64 entries (ST)
- Load Miss Queue: 12 entries
- Store Queue: 80 entries (SMT), 40 entries (ST)
- Prefetch: 16 streams

- TLB: 64 entry
- ERAT: 64 entry

Capacity vs. POWER9:
- Improved
- >= 2x
- = 4x

IBM POWER10
Powerful Core: Enterprise Strength

- Double SIMD + Inference acceleration
  - 2x SIMD, 4x MMA, 4x AES/SHA
- Larger working-sets
  - 1.5x L1-Instruction cache, 4x L2, 4x TLB
- Deeper/wider instruction windows

P10 Core Micro-architecture
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Predecode + Fusion/Prefix

Fetch / Branch Predictors
- I-EA
- L1 Instr. Cache
  - 48k 6-way
  - <EA Tagged>
- 8 instr

Instruction Table
- 512 entries

Instruction Buffer
- 128 entries

Decode/Fuse 8 iop

Execution Slice
- 20 entries
- 128b

MMA Accelerator
- 2x512b

Load Queue
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L2 Cache
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- 48 entries

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- 64 entry

TLB
- 4k entry

TLB miss

L3 prefetch

I miss

D miss

Prefetch
- 16 streams

2 Load EA

2 Store EA

I-EA

32B LD

32B LD

32B ST (+gathered)

64B dedicated

1.5x L1-Instruction cache, 4x L2, 4x TLB

Improved

>= 2x

= 4x

IBM POWER10
Powerful Core: Enterprise Strength

- Double SIMD + Inference acceleration
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- Data latency (cycles)
  - L2 13.5 (minus 2), L3 27.5 (minus 8)
  - L1-D cache 4 +0 for Store forward (minus 2)
  - TLB access +8.5 (minus 7)

IBM POWER10

P10 Core Micro-architecture
½ SMT8 Core Resources Shown = SMT4 Core Equivalent

Fetch / Branch Predictors → I-EA → L1 Instr. Cache 48k 6-way
  <EA Tagged> 8 instr
  → Decode/Fuse 8 iop
  → Instruction Buffer 128 entries
  → Instruction Table 512 entries
  → MMA Accelerator 2x512b
  → Execution Slice 128b
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  → Execution Slice 128b

Load Queue 128 entries (SMT) 64 entries (ST)
  → 2 Load EA
  → Load Miss Queue 12 entries
  → Prefetch 16 streams
  → 2 Store EA
  → L1 Data Cache 32k 8-way
  <EA Tagged>
  → Store Queue 80 entries (SMT) 40 entries (ST)
  → ERAT 64 entry
  → TLB 4k entry
  → 64B dedicated
  → 32B ST (+gathered)
  → TLB miss
  → L3 prefetch
  → L3 Prefetch 48 entries

Predecode +Fusion/Prefix

Capacity vs. POWER9: Improved >= 2x = 4x
Powerful Core: Enterprise Strength

- **Double SIMD + Inference acceleration**
  - 2x SIMD, 4x MMA, 4x AES/SHA
- **Larger working-sets**
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- **Branch**
  - Target registers with GPR in main regfile
  - New predictors: target and direction, 2x BHT

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**P10 Core Micro-architecture**

½ SMT8 Core Resources Shown = SMT4 Core Equivalent

**Fetch / Branch Predictors**

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  - 32B

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  - Decode/Fuse 8 iop

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  - 512 entries

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  - 2x512b

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  - 16 streams

- **Store Queue**
  - 80 entries (SMT), 40 entries (ST)

- **Store Queue**
  - 2 Store EA

- **ERAT**
  - 64 entry

- **TLB**
  - 4k entry

- **L1 Data Cache**
  - 32k 8-way <EA Tagged>

- **L2 Cache**
  - (hashed index)

- **L3 Prefetch**
  - 48 entries

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**Capacity vs. POWER9:**

- Improved
- >= 2x
- = 4x

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IBM POWER10
Powerful Core: **Enterprise Strength**

- **Double SIMD + Inference acceleration**
  - 2x SIMD, 4x MMA, 4x AES/SHA
- **Larger working-sets**
  - 1.5x L1-Instruction cache, 4x L2, 4x TLB
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  - Target registers with GPR in main regfile
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- **Fusion**
  - Fixed, SIMD, other: merge and back to back
  - Load, store: consecutive storage

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**P10 Core Micro-architecture**

1/2 SMT8 Core Resources Shown = SMT4 Core Equivalent

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**IBM POWER10**

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**Capacity vs. POWER9:**

- **Improved**
- **>= 2x**
- **= 4x**
Powerful Core: Energy Efficient

- Double SIMD + Inference acceleration
  - 2x SIMD, 4x MMA, 4x AES/SHA
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- Branch
  - Target registers with GPR in main regfile
  - New predictors: target and direction, 2x BHT
- Fusion
  - Fixed, SIMD, other: merge and back to back
  - Load, store: consecutive storage
- Improved clock-gating
- Design & micro-arch efficiency

Watt vs. POWER9: Improved
Powerful Core: Energy Efficient

- **Double SIMD + Inference acceleration**
  - 2x SIMD, 4x MMA, 4x AES/SHA
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- **Improved clock-gating**
- **Design & micro-arch efficiency**
- **Branch accuracy: less wasted work**
- **Fusion / gather: less units of work**
- **Reduced ports / access**
  - Sliced target reg-file
  - Reduced read ports / entry

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**P10 Core Micro-architecture**

½ SMT8 Core Resources Shown = SMT4 Core Equivalent
**Powerful Core: Energy Efficient**

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  - Reduced read ports / entry
- **EA-tagged L1-D Cache & L1-I Cache**
  - CAM with cache-way/index
  - ERAT only on cache miss

**P10 Core Micro-architecture**

½ SMT8 Core Resources Shown = SMT4 Core Equivalent

- **Fetch / Branch Predictors**
- **Instruction Table** 512 entries
- **Instruction Buffer** 128 entries
- **L1 Instr. Cache** 48k 6-way
  - <EA Tagged>
- **Instruction Table**
- **Execution Slice** 128b
- **Execution Slice** 128b
- **Execution Slice** 128b
- **Execution Slice** 128b
- **Load Queue**
  - 128 entries (SMT)
  - 64 entries (ST)
- **Load Miss Queue**
  - 12 entries
- **Prefetch** 16 streams
- **L1 Data Cache** 32k 8-way
  - <EA Tagged>
- **Store Queue**
  - 80 entries (SMT)
  - 40 entries (ST)
- **32B LD**
- **ERAT**
  - 64 entry
- **L1 Inst. Cache**
  - 8 instr
- **Decode/Fuse** 8 iop
- **L2 Cache**
  - (hashed index)
- **L3 Prefetch** 48 entries
- **Prefetch** 16 streams
- **ERAT** 64 entry
- **TLB** 4k entry
- **TLB miss**
- **L3 prefetch**
- **Watt vs. POWER9: Improved**

IBM POWER10
**Powerful Core : Strength & Efficiency**

- **Improved clock-gating**
- **Design & micro-arch efficiency**
- **Branch accuracy: less wasted work**
- **Fusion / gather: less units of work**
- **Reduced ports / access**
  - Sliced target reg-file
  - Reduced read ports / entry
- **EA-tagged L1-D Cache & L1-I Cache**
  - CAM with cache-way/index
  - ERAT only on cache miss

**Improved**

- Double SIMD + Inference acceleration
  - 2x SIMD, 4x MMA, 4x AES/SHA
- Larger working-sets
  - 1.5x L1-Instruction cache, 4x L2, 4x TLB
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- Fusion
  - Fixed, SIMD, other: merge and back to back
  - Load, store : consecutive storage

### IBM POWER10

**P10 Core Micro-architecture**

\[ \frac{1}{2} \text{SMT8 Core Resources Shown} = \text{SMT4 Core Equivalent} \]

- **Fetch / +Branch Predictors**
- **I-EA**
- **L1 Instr. Cache**
  - 48k 6-way
  - \(<\text{EA Tagged}>\)
- **Instruction Buffer**
  - 128 entries
- **Decode/Fuse 8 iop**
- **MMA Accelerator**
  - 2x512b
- **L1 Data Cache**
  - 32k 8-way
  - \(<\text{EA Tagged}>\)
- **Store Queue**
  - 80 entries (SMT)
  - 40 entries (ST)
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- **ERAT**
  - 64 entry
- **TLB**
  - 4k entry
- **L2 Cache**
  - (hashed index)
- **L3 Prefetch**
  - 48 entries
- **Predecode**
  - +Fusion/Prefix

**Capacity vs. POWER9:**

- **Improved**
- \( \geq 2x \)
- \( = 4x \)
Powerful Core: **Strength & Efficiency**

- **PERFORMANCE**:
  - Double SIMD + Inference acceleration
    - 2x SIMD, 4x MMA, 4x AES/SHA
  - Larger working-sets
    - 1.5x L1-Instruction cache, 4x L2, 4x TLB
  - Deeper/wider instruction windows
  - Data latency (cycles)
    - L2 13.5 (minus 2), L3 27.5 (minus 8)
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    - Target registers with GPR in main regfile
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  - Fusion
    - Fixed, SIMD, other: merge and back to back
    - Load, store: consecutive storage

- **WATT**:
  - Improved clock-gating
  - Design & micro-arch efficiency
  - Branch accuracy: less wasted work
  - Fusion / gather: less units of work
  - Reduced ports / access
    - Sliced target reg-file
    - Reduced read ports / entry
  - EA-tagged L1-D Cache & L1-I Cache
    - CAM with cache-way/index
    - ERAT only on cache miss

---

$$\frac{1.3x}{0.5x} = 2.6x \text{ performance / watt}$$

POWER10 vs. POWER9 Core
Powerful Core: AI Infused Bandwidth and Compute

2x Bytes from all sources
(OMI, L3, L2, L1 caches*)

* versus POWER9
Powerful Core: AI Infused Bandwidth and Compute

2x Bytes from all sources (OMI, L3, L2, L1 caches*)

- 4 32B loads, 2 32B stores per SMT8 Core
  - New ISA or fusion
  - Thread max 2 32B loads, 1 32B store

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  - 256 GB/s peak, 120 GB/s sustained
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4-32x Matrix Math Acceleration*
- 4 512b engines per core = 2048b results / cycle
  - Matrix math outer products: \( A \leftarrow \{\pm\}A \{\pm\}XY^T \)
  - Double, Single, Reduced precision

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### 2x Bandwidth matched SIMD*

<table>
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<tr>
<th>Rank</th>
<th>Operand Type ((X,Y))</th>
<th>Accumulator</th>
<th>Peak [FL]OPS / cycle</th>
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<tbody>
<tr>
<td>1</td>
<td>Float-64 DP (4 \times 1 \times 2)</td>
<td>4\times2 ((\text{Fp-64}))</td>
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<td>Float-32 SP (4 \times 1 \times 4)</td>
<td>(4\times4 ((\text{Fp-32}))</td>
<td>32 64 128</td>
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<td>Int-16 (4 \times 2 \times 4)</td>
<td>(4\times4 ((\text{Int}))</td>
<td>128 256 512</td>
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<tr>
<td>4</td>
<td>Int-8 (4 \times 4 \times 4)</td>
<td>(4\times4 ((\text{Int-32}))</td>
<td>256 512 1024</td>
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<tr>
<td>8</td>
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AI Infused Core: Inference Acceleration

• 4x+ per core throughput
• 3x → 6x thread latency reduction (SP, int8)*

• POWER10 Matrix Math Assist (MMA) instructions
  • 8 512b architected Accumulator (ACC) Registers
  • 4 parallel units per SMT8 core

• Consistent VSR 128b register architecture
  • Minimal SW ecosystem disruption – no new register state
  • Application performance via updated library (OpenBLAS, etc.)
  • POWER10 aliases 512b ACC to 4 128b VSR’s
    • Architecture allows redefinition of ACC

• Dense-Math-Engine microarchitecture
  • Built for data re-use algorithms
  • Includes separate physical register file (ACC)
  • 2x efficiency vs. traditional SIMD for MMA

* versus POWER9

Inference Accelerator dataflow (2 per SMT8 core)
POWER10 SIMD / AI Socket Performance Gains

(Performance assessments based upon pre-silicon engineering analysis of POWER10 dual-socket server offering vs POWER9 dual-socket server offering)