

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TOSHIBA CORPORATION,
Petitioner,

v.

INTELLECTUAL VENTURES II LLC,
Patent Owner.

Case IPR2014-00317
Patent 5,687,132

Before KEVIN F. TURNER, TREVOR M. JEFFERSON,
and DAVID C. McKONE, *Administrative Patent Judges*.

McKONE, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. *Background*

Toshiba Corporation, Toshiba America, Inc., Toshiba America Electronic Components, Inc., and Toshiba America Information Systems, Inc. (collectively, “Petitioner”) filed a Petition (Paper 1, “Pet.”) to institute an *inter partes* review of claims 1–14 and 28–30 of U.S. Patent No. 5,687,132 (Ex. 1001, “the ’132 patent”). *See* 35 U.S.C. § 311. Intellectual Ventures II LLC (“Patent Owner”) filed a Preliminary Response (Paper 9, “Prelim. Resp.”). Pursuant to 35 U.S.C. § 314, in our Decision to Institute (Paper 11, “Dec.”), we instituted this proceeding as to claims 1–14, 28, and 29.

After the Decision to Institute, Patent Owner filed a Patent Owner Response (Paper 20, “PO Resp.”) and Petitioner filed a Reply to the Patent Owner Response (Paper 25, “Reply”). An oral hearing (Paper 33, “Tr.”) was held on March 17, 2015.

B. *Related Cases*

Patent Owner has asserted the ’132 patent against Petitioner in *Intellectual Ventures I LLC & Intellectual Ventures II LLC v. Toshiba Corp.*, Case No. 1:13-cv-00453 (D. Del.). Pet. 1; Paper 5, at 2. Patent Owner also has asserted the ’132 patent in *Intellectual Ventures I LLC & Intellectual Ventures II LLC v. Hynix Semiconductor*, Case No. 2:11-cv-01145 (W.D. Wash.). Paper 5, at 2.

The ’132 patent was under *ex parte* reexamination, Control Number 90/012,571 (“the ’571 reexam”). Pet. 1. Prior to our Decision to Institute,

the Examiner in the '571 reexam mailed a Notice of Intent to Issue *Ex Parte* Reexamination Certificate ("NIRC") confirming claims 1, 2, 4, 6, 9, 10, 28, and 29.¹ Ex. 2001, at 3. Specifically, the Examiner concluded that each of the claims under reexamination includes a requirement of a single memory, rather than two separate memories, a limitation the Examiner found lacking in the cited prior art (which includes references that overlap with those raised in the Petition). *Id.* at 10–11. After our Decision to Institute, the Office issued an *Ex Parte* Reexamination Certificate, US 5,687,132 C1, confirming claims 1, 2, 4, 6, 9, 10, 28, and 29.

C. References Relied Upon

Petitioner relies upon the following prior art references:

Ex. 1004	Konishi	US 6,170,036 B1	Jan. 2, 2001 (filed Oct. 25, 1991)
Ex. 1005	Fujishima	US 5,353,427	Oct. 4, 1994

D. The Asserted Grounds

We instituted this proceeding based on the grounds of unpatentability set forth in the table below. Dec. 29.

References	Basis	Claims Challenged
Konishi	35 U.S.C. § 102(e)	1–14, 28, and 29
Fujishima	35 U.S.C. § 102(b)	1–12, 28, and 29

¹ The remaining claims of the '132 patent were not subject to reexamination. Ex. 2001, at 3.

E. The '132 Patent

The '132 patent is directed to multiple-bank computer memories. Ex. 1001, 1:6–8. In one example, a memory includes an array of memory cells divided into multiple subarrays. *Id.* at 3:4–9. The bitlines of the first subarray are coupled selectively to the bitlines of the second subarray by gating circuitry. *Id.* Figure 2A, reproduced below, is illustrative:

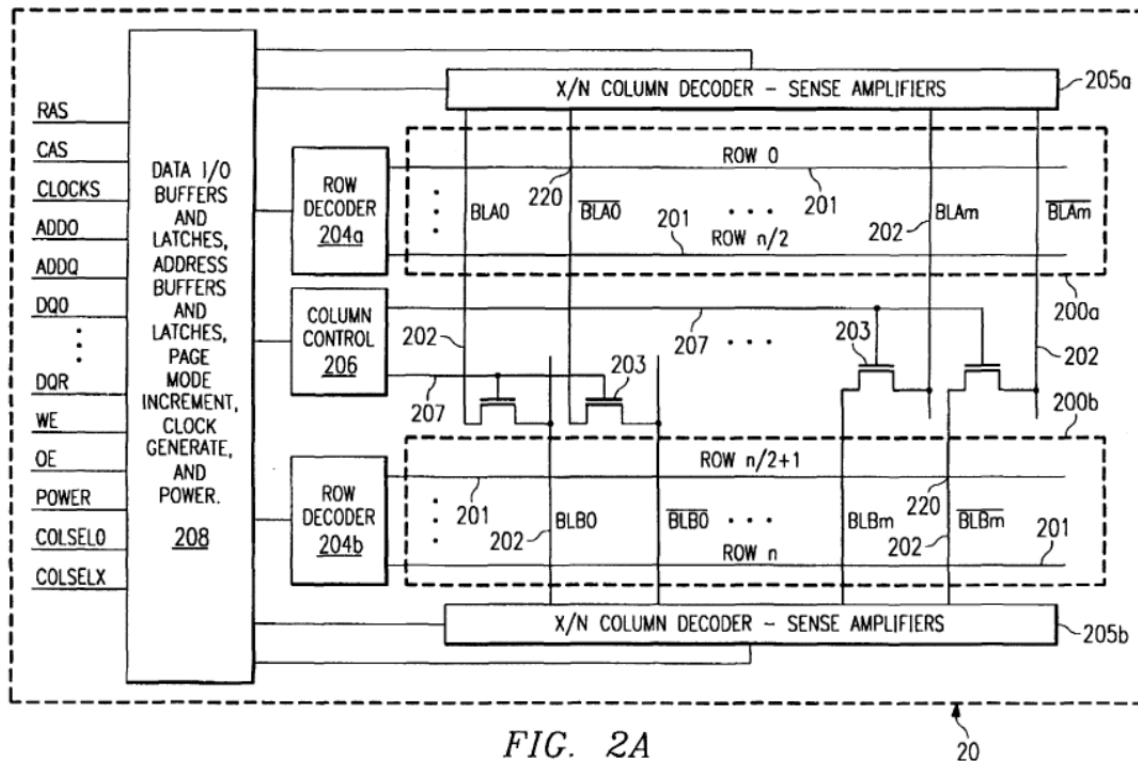


Figure 2A is a functional block diagram of memory 20. *Id.* at 7:5–6. Memory 20 includes a plurality of rows and columns of dynamic random access memory (“DRAM”) cells partitioned into upper subarray 200a and lower subarray 200b. *Id.* at 7:10–16. Rows of cells are accessed using conductive wordlines (such as ROW 0 through ROW n/2 of upper subarray 200a and ROW n/2+1 through ROW n of lower subarray 200b) under the

control of row decoders (such as ROW DECODER 204a for upper subarray 200a and ROW DECODER 204b for lower subarray 200b). *Id.* at 7:39–46. Columns are arranged as pairs of bitlines (such as BLAm and $\overline{\text{BLAm}}$ for upper subarray 200a and BLBm and $\overline{\text{BLBm}}$ for lower subarray 200b). *Id.* at 7:47–59.

Bitlines in the upper subarray can be coupled to bitlines in the lower subarray using gates 203 under the control of column control circuitry 206. *Id.* at 8:45–47. For example, information in cells of upper subarray 200a can be transferred during a single gate delay to cells of lower subarray 200b by controlling gates 203 to couple bitlines BLAm and $\overline{\text{BLAm}}$ to BLBm and $\overline{\text{BLBm}}$. *Id.* at 8:47–51.

According to the '132 patent, the ability to transfer blocks of data between arrays of memory cells quickly is advantageous for computers driving multiple asynchronous display devices. *Id.* at 12:15–24.

Claim 1, reproduced below, is illustrative of the claimed subject matter:

1. A memory comprising:
 - a first plurality of columns of memory cells each including at least one conductive bitline;
 - a second plurality of columns of memory cells each including at least one conductive bitline; and
 - a plurality of gates organized in independently controlled groups for selectively coupling said bitlines of a selected group of said first plurality of columns with a group of said bitlines of said second plurality of columns for transferring a at least one bit of data

from a selected cell of said first plurality of columns of cells to a selected cell of said second plurality of columns of cells.

II. ANALYSIS

A. *Claim Construction*

The Board interprets claims of an unexpired patent using the broadest reasonable construction in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b); *In re Cuozzo Speed Techs., LLC*, 778 F.3d 1271, 1279–81 (Fed. Cir. 2015). Claim terms generally are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

1. “*first subarray*” / “*second subarray*”

Independent claim 6 recites a “memory system” comprising “a first subarray of memory cells” and “a second subarray of memory cells.” Dependent claim 4 and independent claim 28 similarly recite “a first subarray” and “a second subarray.” In the Decision to Institute, we preliminarily construed “first subarray” to mean “a first memory cells partition including a plurality of rows and columns of memory cells” and “a second subarray” to mean “a second memory cells partition including a

plurality of rows and columns of memory cells.” Dec. 10.² As explained in the Decision to Institute (at 9), the ’132 patent describes an example memory that “includes an array of n number of rows and m number of columns of memory cells partition[ed] into an upper bank or subarray 200a and a lower bank or subarray 200b.” Ex. 1001, 7:10–12. Thus, the ’132 patent supports a construction in which a subarray is a memory cells partition including a plurality of rows and columns of memory cells.

Patent Owner disagrees with our preliminary construction and contends that a “first subarray of memory cells” and a “second subarray of memory cells,” together, are “memory cell partitions, in which the partitions have the same type of memory cells as one another.” PO Resp. 15 (emphasis omitted). Patent Owner supports its argument with the testimony of William R. Huber, D.Sc., P.E. (Ex. 2002, “Huber Decl.”).

Patent Owner first argues that its proposal is supported by the plain and ordinary meaning of the claim language. According to Patent Owner, first and second subarrays necessarily are “sub” parts of a parent memory array and, accordingly, must have common characteristics. PO Resp. 15–16. This argument is not persuasive, however, as the claim language does not specify that the two subarrays comprise memory cells from a single parent

² In the Decision to Institute, we construed the terms “a first subarray” and “a second subarray,” which appear in claims 4, 6, and 28. Patent Owner proposes constructions for “a first subarray of memory cells” and “a second subarray of memory cells,” terms that appear in claims 6 and 28, but not claim 4. Nevertheless, Patent Owner makes similar arguments regarding the applicability of the prior art to claim 4, which recites “memory cells forming a first subarray” and “cells forming a second subarray.” To make clear that our constructions apply to each of claims 4, 6, and 28, we construe the terms “a first subarray” and “a second subarray.”

array. For example, a memory subsystem comprising a first subarray of memory cells of a first array (a “sub” of the first array) and a second subarray of memory cells of a second array (a “sub” of the second array) is consistent with the plain language of claim 6.

Patent Owner also argues that its proposed constructions are more consistent with the manner in which the ’132 patent describes solving problems experienced with the prior art. Specifically, Patent Owner argues that the ’132 patent identifies prior art systems as inefficient. PO Resp. 3. For example, the ’132 patent states that a block data transfer technique involving the “use of two operations (a read and a write) results in substantial inefficiencies, especially when the transfer crosses chip boundaries.” Ex. 1001, 1:52–67. According to Patent Owner, the invention solves this problem by a technique that uses subarrays of the same type of memory cells. PO Resp. 3–5. Patent Owner points to disclosure in the Specification explaining that “[t]o insure smooth operation, the physical structure of subarrays 200 [shown in Figure 2A, reproduced above] should be substantially identical. Among other things, the cell density, row/column pitch, bitline length (hence bitline capacitance) and number of cells per row and column should be substantially the same.” Ex. 1001, 11:24–28. Patent Owner argues that differences in memory characteristics would prevent smooth operation when transferring data between SRAM and DRAM cells. PO Resp. 7–8.

Petitioner replies that Patent Owner points to the description of a non-limiting example of how the invention “should” be implemented in order to achieve smooth operation rather than how it must be implemented to meet the limitations of claims 4, 6, and 28. Reply 8–9. We agree with Petitioner.

None of claims 4, 6, and 28 recites that both subarrays must have memory cells of the same type. Instead, they more broadly recite “a first subarray” and “a second subarray,” without qualifications. *See In re Am. Academy of Sciences Tech. Ctr.*, 367 F.3d 1359, 1369 (Fed. Cir. 2004) (“We have cautioned against reading limitations into a claim from the preferred embodiment described in the specification, even if it is the only embodiment described, absent clear disclaimer in the specification. “). Patent Owner has not explained persuasively how this example limits claim 6. Notably, Patent Owner concedes that efficiency and smooth operation are not requirements of the claims. Tr. 33:7–34:5.

Moreover, Patent Owner seeks to read limitations into the claims from the Specification selectively. For example, the Specification explains that “[s]mooth operation is also insured in embodiments using the folded bitline arrangement described above.” Ex. 1001, 11:28–30. By Patent Owner’s rationale, the claims also should be construed to require folded bitline arrangements. Nevertheless, Patent Owner argues that a folded bitline arrangement is not required by the claims. Tr. 49:19–50:13. We conclude that similarity in memory structure and folded bitline arrangements are both non-limiting examples of ways to improve efficiency of data transfer.

Patent Owner further argues that the Specification of the ’132 patent consistently describes the two subarrays as having the same type of memory cells. PO Resp. 16–19. For example, according to the Specification, with reference to Figure 2A (reproduced above), “[m]emory 20 includes an array of n number of rows and m number of columns of memory cells partition[ed] into an upper bank or subarray 200a and a lower bank or subarray 200b.” Ex. 1001, 7:10–12. The Specification also describes an example in which it

is assumed that “data is to be exchanged between subarrays in 64-bit blocks (64 bitline pairs or 128 bitlines) and that each subarray 200 includes 512 column pairs.” *Id.* at 9:28–31. Petitioner concedes that the Specification does not describe any examples in which the two subarrays have different types of memory cells. Tr. 11:18–23.

Dr. Huber testifies that, in light of these examples, the Specification “only contemplates the transfer of data between subarrays, where the subarrays include the same type of memory cells” and “does not disclose, nor does it contemplate, the transfer of data between subarrays with different types of memory cells.” Ex. 2002 ¶ 35. Dr. Huber, however, does not cite evidence other than the Specification itself, for this conclusion, nor does he provide persuasive explanation why the Specification is limited to the described examples. We conclude that the examples described in the Specification do not evidence a clear disclaimer of subarrays with different types of memory cells. *See Am. Academy*, 367 F.3d at 1369.

Patent Owner also argues that the Specification effectively defines subarrays as having the same type of memory cells by describing the subarrays as “banks.” PO. Resp. 20; *see also, e.g.*, Ex. 1001, 7:10–12 (“Memory 20 includes an array of n number of rows and m number of columns of memory cells partition[ed] into an *upper bank or subarray* 200a and a *lower bank or subarray* 200b.” (emphases added)). According to Patent Owner and Dr. Huber, at the time the application leading to the ’132 patent was filed, the term “bank” referred to a partition of a memory array, and a skilled artisan would have understood “multibank memory system” to mean a system with memory banks having the same type of memory cells. PO Resp. 20–21; Ex. 2002 ¶¶ 37, 40–42.

Claims 4, 6, and 28 do not recite the term “bank.” Rather, they use the term “subarray.” To the extent that “bank” is narrower than “subarray,” we do not read Patent Owner’s citations to the Specification as defining a subarray to be a bank or otherwise limiting the term “subarray” to examples in which banks are described. Patent Owner relies on the statement in the Specification that “[i]n general, the principles of the present invention provide for the construction and operation of multiple bank memories,” Ex. 1001, 3:2–4, arguing that this is a statement of the invention. Tr. 27:9–15. Again, however, Patent Owner seeks to limit the claims to the Specification selectively. The Specification continues “the principles of the present invention allow for the two banks of memory to be operated asynchronously and independently.” Ex. 1001, 3:13–15. Patent Owner argues that this second statement of the principles of the invention is not limiting, attempting to draw a distinction between the language “provide for” and “allow for.” Tr. 29:21–31:2. Patent Owner’s distinction is not persuasive. We conclude that both of the statements of the principles of the invention are examples that do not limit the claims.

Moreover, we are not persuaded by Patent Owner’s extrinsic evidence that memory “banks” are limited to memory cells of the same type. To show how a skilled artisan would have understood the term “bank,” Patent Owner and Dr. Huber rely on two textbooks, BETTY PRINCE, HIGH PERFORMANCE MEMORIES, NEW ARCHITECTURE DRAMS AND SRAMS EVOLUTION AND FUNCTION (1996) (Ex. 2004, “Prince 1996”), and BETTY PRINCE, SEMICONDUCTOR MEMORIES, A HANDBOOK OF DESIGN, MANUFACTURE, AND APPLICATION (2nd ed. 1991) (Ex. 2005, “Prince 1991”). PO Resp. 21–22; Ex. 2002 ¶¶ 37, 40–41. For example, Prince 1996 describes that “[a]n

additional speed advantage sported by the JEDEC Standard Synchronous DRAM and the Rambus DRAM is multiple banks on a single RAM.” Ex. 2004, at 9; *see also id.* at 210 (illustrating a Mosys DRAM chip concept solving certain problems “by integrating many small DRAM banks onto a single chip all connected to a fast common bus internal to the chip and controlled on chip for clock skew.”). In Prince 1991, Patent Owner points to Figure 7.40(b), which it contends shows an on-chip interleaved circuit with multiple memory banks of the same type of memory cell. PO Resp. 21–22 (citing Ex. 2005, at 363); Ex. 2002 ¶ 40 (same). We agree that both Prince 1996 and Prince 1991 include examples in which multiple banks of memory have the same type of memory cells. Nevertheless, we find that neither extrinsic source defines “bank” or describes memory banks in a manner that would exclude banks of different types of memory cells.

Patent Owner also points to the background section of Konishi (a prior art reference discussed below) as describing a DRAM memory with multiple memory banks of the same type of memory cell. PO Resp. 23–25. According to Konishi, “[i]n most MPU systems, the memories are adopted to have bank structure and interleaving is carried out on [a] bank by bank basis” Ex. 1004, 2:61–63. Konishi’s background describes a technique that “is effective to some extent when the number of banks is comparatively larger, for example 2 to 4,” but notes that “it is not practical to provide 30 to 40 banks in a data processing system.” *Id.* at 3:6–22. Patent Owner acknowledges that Konishi also describes an embodiment (Figure 5) that includes both DRAM and SRAM cells. PO Resp. 25 n.5. Patent Owner distinguishes this embodiment as not using the term “bank” or “subarray,” arguing that this means it is not a multibank system. *Id.* Dr. Huber, in turn,

provides testimony that the absence of the word “bank” in describing the Figure 5 embodiment is “revealing” that multibank memories do not include memory cells of different types. Ex. 2002 ¶ 43. Dr. Huber’s conclusory testimony does not provide persuasive explanation as to why we should understand Konishi’s Figure 5 embodiment to be a departure from the prior art use of memory banks rather than an improvement thereon. *Cf.* Ex. 1004, 7:46–48 (“Another object of the present invention is to provide an improved semiconductor memory device containing a cache which can realize a desired mapping system easily.”). In any case, as with Prince 1996 and Prince 1991, Konishi’s background does not define “bank” or describe memory banks as limited to memory cells of the same type. In short, there is no dispute that two banks of memory *can* be of the same type of memory cell. Nevertheless, Patent Owner’s extrinsic sources present no evidence that two banks of memory *must* be of the same type of memory cell.

In sum, the ’132 patent Specification describes examples of subarrays that are of the same type of memory cells and in some instances uses the term “bank” to refer to a subarray. Nevertheless, these are just examples and, under a broadest reasonable interpretation, are not limitations that should be read into the claims. Patent Owner’s extrinsic evidence, including Dr. Huber’s testimony, does not persuade us otherwise. Accordingly, on the full record, we maintain our constructions of “first subarray” as meaning “a first memory cells partition including a plurality of rows and columns of memory cells” and “a second subarray” as meaning “a second memory cells partition including a plurality of rows and columns of memory cells.”

2. “a memory” and “a memory subsystem”

In the Decision to Institute, we preliminarily construed “a memory,” recited in claim 1, to mean “one or more memories.” Dec. 8. Likewise, we preliminarily construed “a memory subsystem,” recited in claims 6 and 28, to mean “one or more memory subsystems.” *Id.* at 8–9. We relied on Federal Circuit precedent

repeatedly emphas[ing] that an indefinite article “a” or “an” in patent parlance carries the meaning of “one or more” in open-ended claims containing the transitional phrase “comprising.” That “a” or “an” can mean “one or more” is best described as a rule, rather than merely as a presumption or even a convention. The exceptions to this rule are extremely limited: a patentee must “evinced [] a clear intent” to limit “a” or “an” to “one.”

Baldwin Graphic Sys., Inc. v. Siebert, Inc., 512 F.3d 1338, 1342 (Fed. Cir. 2008) (internal citations and quotation marks omitted). Applying this rule, we determined that the ordinary meaning of “a memory” is “one or more memories.” Dec. 7–8.

While Patent Owner presented citations to the Specification giving examples in which two subarrays of memory cells were included on the same physical chip (Ex. 1001, 3:7–9, 7:10–12), we noted that this disclosure was qualified by a statement in the Specification that “the present invention is not limited to single chip embodiments” (*id.* at 7:6–9).

Patent Owner advances the same evidence in its PO Response, again arguing that “a memory” is “a single memory and not the combination of two different memories” and that “a memory subsystem” is “a subsystem providing a single memory and not a subsystem providing two different memories.” PO Resp. 27–28 (emphasis omitted). At the hearing, Patent Owner argued that we misapplied *Baldwin* and should have given more

weight to the Specification. Tr. 52:19–54:2. As explained above, however, we specifically considered the Specification’s statement that the invention is not limited to single chip embodiments. Ex. 1001, 7:6–9. Even Dr. Huber acknowledges that “the present invention is not limited to a single chip embodiment.” Ex. 2002 ¶ 31. For the first time at the hearing, Patent Owner argued that the Specification really means that “you would separate control circuitry for memory and put that on a chip and you keep that -- the arrays together on a different chip. That’s the multichip embodiment.” Tr. 43:23–44:6. Patent Owner offers no persuasive evidence to support this argument, nor do we find any such description in the Specification.

Patent Owner further argues that “a memory” and “a memory subsystem” are limited to memories or subsystems that have “a single type of memory cells or the same type of memory cells.” PO Resp. 28 (emphasis omitted). For the reasons given above for “a first subarray” and “a second subarray,” we are not persuaded that the Specification or the extrinsic evidence supports reading such a limitation into the claims.

On the full record, we maintain our constructions of “a memory” as meaning “one or more memories” and “a memory subsystem” as meaning “one or more memory subsystems.”

3. The ’571 reexam

As explained above, claims 1, 2, 4, 6, 9, 10, 28, and 29 of the ’132 patent were confirmed during reexamination. At the time of our Decision to Institute, the Examiner in the ’571 reexam had issued a NIRC confirming those claims. Ex. 2001. In the Preliminary Response, Patent Owner argued that we should reject the Petition based on 35 U.S.C. § 325(d), which gives

us discretion to “take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office.” Prelim. Resp. 1. We declined to exercise that discretion, citing our disagreement with the Examiner’s claim construction in the NIRC. Dec. 3. Following our Decision on Institution, the Office issued a Reexamination Certificate, US 5,687,132 C1, confirming claims 1, 2, 4, 6, 9, 10, 28, and 29.

Patent Owner again contends that the reexamination decision supports its proposed constructions of “a first subarray of memory cells,” “a second subarray of memory cells,” “a memory,” and “a memory subsystem,” arguing that the Examiner effectively adopted the constructions Patent Owner proposes in this proceeding. PO Resp. 31–34. We are not persuaded.

As detailed in the NIRC, the Examiner considered, and agreed with, Patent Owner’s argument that “a memory” and “a memory subsystem” are limited to a single memory or single memory subsystem, respectively. Ex. 2001, at 9–10 (“Even though the claim only recited ‘a memory’ not ‘a single memory’; . . . However, it is agreed that the prior art references of record fail to teach or suggest the combination of the claimed limitations, for example: the first plurality of columns of memory cells and the second plurality of columns of memory cells are located in a same memory . . . ; or a first subarray of memory cells and a second subarray of memory cells are located in a same memory subsystem . . .”). For the reasons given in Section II.A.2 above, and in the Decision to Institute, at 7–8, we continue to disagree with the Examiner’s construction in the NIRC. Accordingly, we do not adopt it in this proceeding.

Patent Owner argues that the Examiner also considered, and adopted, its proposed requirement that the recited memory, memory subsystem, first subarray, and second subarray have the same type of memory cells. PO Resp. 32–33. The record does not show that this argument was presented to, or accepted by, the Examiner in the '571 reexam. *See, e.g.*, Ex. 1003 (Nov. 1, 2013, Patent Owner Response in '571 reexam), at 106 (arguing that the claims require a single memory or memory subsystem or subarrays from a same memory or memory subsystem). Thus, Patent Owner's argument that the Office already considered and adopted this proposed construction is not persuasive.

4. “folded bitlines”

In the Decision to Institute we preliminarily construed “folded bitlines” to mean “a pair of bitlines, one for carrying ‘true logic’ data and the other for carrying the complement of that data.” Dec. 10–11. We based our construction on the '132 patent's description that “[i]n the preferred embodiment, the columns of cells are arranged as pairs of folded bitlines 202, one for carrying ‘true logic’ data from a selected cell and the other for carrying the complement of that data.” *Id.* (quoting Ex. 1001, 7:47–50).

Patent Owner contends that our preliminary construction was too broad in that it encompasses open bitline configurations. PO Resp. 30–31. Rather, Patent Owner argues, “folded bitlines” should be construed to mean “bitlines (e.g., carrying ‘true’ and complement data) routed generally in parallel with one another.” *Id.* at 29. Patent Owner relies on a pair of figures from Prince 1991, one showing an open bit-sense line and another showing folded bit-lines. *Id.* at 29–30 (citing Ex. 2005, at 231). While this

evidence provides an example of a folded bitline configuration, Patent Owner does not point to any definition excluding open bitline configurations. Patent Owner also cites to Dr. Huber (Ex. 2002 ¶ 53), but that testimony simply repeats the arguments in the PO Response.

Petitioner faults Patent Owner for relying on extrinsic evidence rather than intrinsic evidence, but does not address directly Patent Owner's evidence. Reply 12. As Petitioner notes (*id.*), however, Patent Owner does not distinguish any claim of the '132 patent from the cited prior art based on its construction of "folded bitlines."

Patent Owner has presented evidence sufficient to cast doubt on the reasonableness of our preliminary construction of folded bitlines but has not introduced evidence persuasively supporting its own proposed construction. Because the construction of "folded bitlines" does not affect the outcome of this proceeding, we vacate our preliminary construction and decline to construe this term expressly for purposes of this Decision.

B. Anticipation by Konishi

Petitioner contends that Konishi anticipates claims 1–14, 28, and 29. Petitioner supports its contentions with the testimony of Robert Murphy (Ex. 1008, "Murphy Decl.").

1. Overview of Konishi

Konishi describes a semiconductor memory device with a static random access memory ("SRAM") array, a DRAM array, and an internal data line that enables the transfer of data blocks between the SRAM array

and the DRAM array. Ex. 1004, Abstract. This is illustrated in Figure 6, reproduced below:

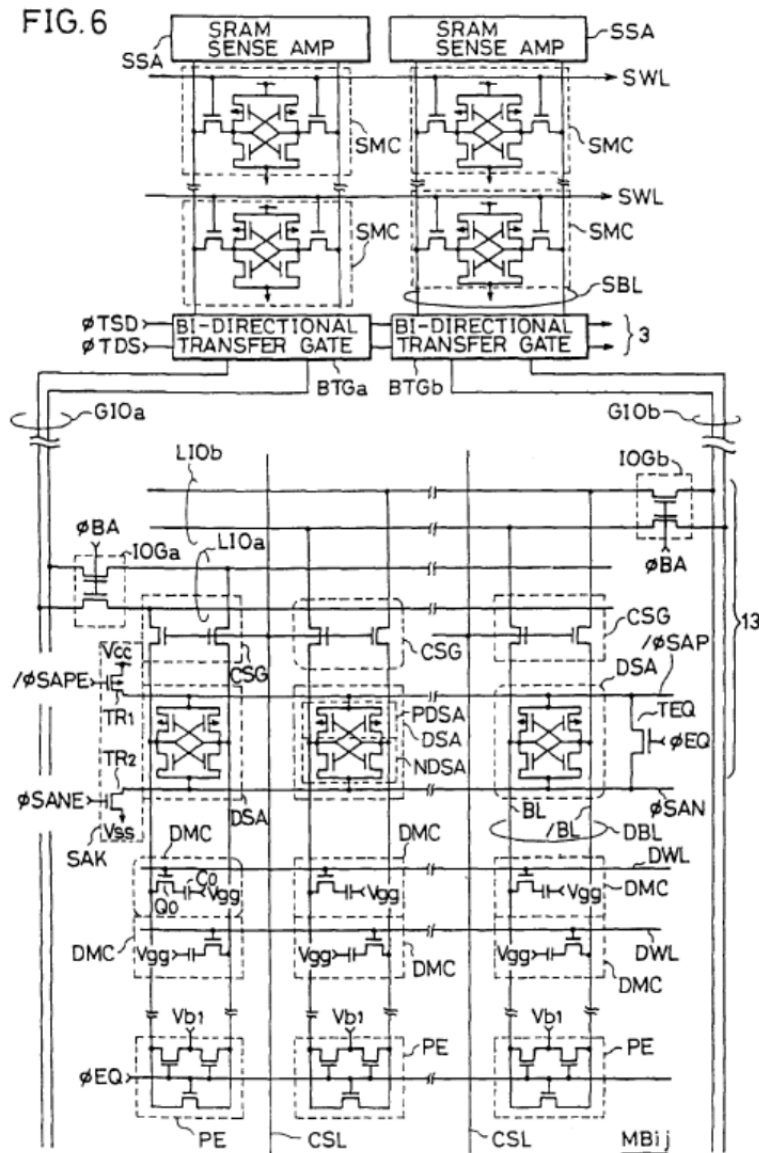


Figure 6 shows the detailed structure of the portions of the SRAM and DRAM arrays related to one block of a semiconductor memory device. *Id.* at 9:16–18, 15:39–43.

As shown in Figure 6, a DRAM array includes a plurality of DRAM cells DMC arranged in rows and columns and an SRAM array includes a plurality of SRAM cells SMC arranged in rows and columns. *Id.* at 15:43–47, 16:59–65. The DRAM array includes a plurality of word lines DWL, each of which is under the control of row decoder 14 and is connected to one row of DRAM cells DMC. *Id.* at 17:41–51, Fig. 5. The DRAM array also includes a plurality of bitline pairs DBL (also designated BL and /BL), with each pair connected to a column of DRAM cells DMC. *Id.* at 15:48–51. The SRAM array includes a plurality of word lines SWL, each of which is connected to one row of SRAM cells SMC, and a plurality of bitline pairs SBL, with each pair connected to a column of SRAM cells SMC. *Id.* at 16:59–65. SRAM column selection is controlled by column decoder 22 and row selection is controlled by row decoder 21. *Id.* at 14:21–29, Fig. 5.

Each DRAM memory block also includes a column selecting gate CSG for each bitline pair DBL for selecting the column associated with that bitline pair. *Id.* at 16:36–46. The column selecting gates CSG are controlled by activating column selecting lines CSL using a column decoder 15 (shown in Figure 5). *Id.* at 16:36–46, 18:1–4. Additionally, each DRAM memory block includes input/output (“IO” or “I/O”) gates IOGa, IOGb that connect local I/O line pairs LIOa, LIOb to global I/O line pairs GIOa, GIOb. *Id.* at 16:47–50. The SRAM array includes bi-directional transfer gates BTGa, BTGb that transfer data between the SRAM bitline pair SBL and the global I/O line pairs GIOa, GIOb. *Id.* at 16:65–17:8.

Data are transferred between the SRAM and DRAM arrays by selecting appropriate rows and columns (e.g., using word lines SWL and column selecting lines CSL for the DRAM array) and turning on appropriate

gates (IO gates IOGa, IOGb, and bi-directional transfer gates BTGa, BTGb) as shown in Figure 8. *Id.* at 17:20–19:11.

2. *Claims 1–5*

Regarding claim 1, Petitioner contends that:

Konishi's array of DRAM cells DMC is the recited "first plurality of columns of memory cells each including at least one conductive bitline" (Petitioner identifies bitlines BL and /BL);

Konishi's array of SRAM cells SMC is the recited "second plurality of columns of memory cells each including at least one conductive bitline" (Petitioner identifies bitlines SBL); and

gates CSG, IOGa, IOGb, BTGa, and BTGb together constitute a "plurality of gates" for coupling the bitlines of the first plurality of columns to the bitlines of the second plurality of columns for transferring data between those pluralities of columns.

Pet. 17–19. According to Petitioner, each pair of column selecting gates CSG is controlled independently by a unique column selecting line CSL signal and, thus, the CSGs organize independently controlled groups. *Id.* at 17–18.

Patent Owner argues that Konishi does not anticipate claim 1 because it discloses transferring data between memories having different types of memory cells. PO Resp. 35–38, 41–42. As explained in Sections II.A.1 and II.A.2, above, however, "a memory," as recited in claim 1, is not limited to a single memory with the same type of memory cells. Accordingly Patent Owner's argument is not persuasive. Rather, we find that Konishi's DRAM and SRAM, together, constitute "one or more memories," as we have construed "a memory." Patent Owner does not otherwise dispute Petitioner's description of the disclosure of Konishi. Tr. 54:3–6 ("[T]here is

no dispute between the parties relative to how Konishi . . . operate[s]. The parties agree regarding the technical operation[] of . . . Konishi.”).

We have considered the evidence presented by Petitioner and Patent Owner. On the full record, Petitioner has shown by a preponderance of the evidence that Konishi anticipates claim 1.

We also have considered Petitioner’s evidence and argument for claims 2, 3 and 5, which depend from claim 1. Pet. 19–20. For example, regarding claim 5, Petitioner contends that Konishi’s wordlines DWL and SWL are conductive wordlines for the rows of the DRAM and SRAM arrays, respectively, and that row decoder 14 is a first row decoder and row decoder 21 is a second row decoder. Pet. 19–20. Patent Owner does not present separate arguments for claims 2, 3, and 5. PO Resp. 43. On the full record, Petitioner has shown by a preponderance of the evidence that Konishi anticipates claims 2, 3, and 5.

Claim 4 recites “a first subarray” and “a second subarray.” Patent Owner argues that Konishi does not disclose memory cell partitions in which the partitions have the same type of memory cells as one another and, thus, does not anticipate claim 4. PO Resp. 42–43. As explained in Section II.A.1 above, however, “a first subarray” and “a second subarray,” as recited in claim 4, are not limited to partitions with the same type of memory cells. Thus, Patent Owner’s argument is not persuasive.

We find that Konishi’s DRAM array is “a first memory cells partition including a plurality of rows and columns of memory cells” and that Konishi’s SRAM array is “a second memory cells partition including a plurality of rows and columns of memory cells.” We have considered the evidence presented by Petitioner and Patent Owner. On the full record,

Petitioner has shown by a preponderance of the evidence that Konishi anticipates claim 4.

3. Claims 6, 8–10, and 12–14

Regarding independent claim 6, Petitioner contends that:

Konishi's DRAM array, with its associated bitlines DBL and wordlines DWL, is a "first subarray of memory cells arranged in rows and columns, each said column associated with a conductive bitline and each said row associated with a conductive wordline";

Konishi's SRAM array, with its associated bitlines SBL and wordlines SWL is a "second subarray of memory cells arranged in rows and columns, each said column associated with a conductive bitline and each said row associated with a conductive wordline";

Konishi's gates CSG, IOGa, IOGb, BTGa, and BTGb, together, constitute "circuitry for independently coupling selected groups of bitlines of said first subarray with corresponding groups of bitlines of said second subarray";

Konishi's column decoder 15 is a "first column decoder" coupled to the bitlines DBL of the first (DRAM) subarray; and

Konishi's column decoder 22 is a "second column decoder" coupled to the bitlines SBL of the second (SRAM) subarray.

Pet. 20–22.

Patent Owner argues that Konishi does not disclose memory cell partitions in which the partitions have the same type of memory cells as one another and, thus, does not disclose the "first subarray" and "second subarray" of claim 6. PO Resp. 42–43. As explained in Section II.A.1 above, however, "a first subarray" and "a second subarray," as recited in

claim 6, are not limited to partitions with the same type of memory cells. Thus, Patent Owner's argument is not persuasive.

Patent Owner also argues that Konishi does not disclose "a memory subsystem," as recited in claim 6, because it discloses transferring data between memories having different types of memory cells. PO Resp. 35–38, 41–42. As explained in Sections II.A.1 and II.A.2, above, however, "a memory subsystem," as recited in claim 6, is not limited to a single memory with the same type of memory cells. Patent Owner does not otherwise dispute Petitioner's description of the disclosure of Konishi. Tr. 54:3–6.

We have considered the evidence presented by Petitioner and Patent Owner. On the full record, Petitioner has shown by a preponderance of the evidence that Konishi anticipates claim 6.

We also have considered Petitioner's evidence and argument for claims 8–10 and 12–14, which depend from claim 6. Pet. 22–25. For example, regarding claim 8, Petitioner argues that Konishi's DRAM bitline pair DBL, which includes bitlines BL and /BL, is a pair of folded bitlines. Pet. 23. As Petitioner points out, Konishi describes the signals carried on the bitline pair as including signals complementary to each other. *Id.* (citing Ex. 1004, 15:51–56). As shown in Konishi's Figure 6, BL and BL/ are generally parallel to one another. Thus, we are persuaded that bitline pair DBL is a pair of folded bitlines under either party's proposed construction. Patent Owner does not argue claims 8–10 and 12–14 separately. PO Resp. 43. On the full record, Petitioner has shown by a preponderance of the evidence that Konishi anticipates claims 8–10 and 12–14.

4. Claims 7 and 11

Claim 7 depends from claim 6 and recites “column control circuitry operable to cause said circuitry for gating to coupled selected ones of said bitlines in response to a received control signal.” Claim 11 depends from claims 8 and 6 and recites “control circuitry for causing said circuitry for coupling to couple a said bitline and a complementary said bitline of said first subarray with a said bitline and a complementary said bitline of said second subarray in response to a received control signal.” Petitioner identifies signals ϕ BA and ϕ TDS (depicted in Figure 6) as the column control circuitry of claim 7 and the control circuitry of claim 11.

ϕ BA is a block activating signal that activates gates IOGa and IOGb to connect local I/O line pairs LIOa and LIOb to global I/O line pairs GIOa and GIOb, respectively. Ex. 1004, 16:47–50. ϕ TDS is a data transfer designating signal that causes bi-directional transfer gates BTGa and BTGb to transfer data between SRAM bitline pair SBL and global I/O line pairs GIOa and GIOb. *Id.* at 17:1–4. As Konishi states, “data transfer designating signal ϕ TDS designates data transfer from DRAM portion to SRAM portion.” *Id.* at 17:6–8. According to Mr. Murphy, “[a]lthough the circuitry that generates the gating control signals ϕ BA and/or ϕ TDS is not specifically shown in Konishi’s figures, one of skill in the art would understand that circuitry is required to generate these signals.” Ex. 1008 ¶ 21.

Regarding claim 7, Patent Owner does not dispute that ϕ BA and ϕ TDS “cause said circuitry for gating to coupled selected ones of said bitlines in response to a received control signal.” Patent Owner also does not dispute that ϕ BA and ϕ TDS “caus[e] said circuitry for coupling to

couple a said bitline and a complementary said bitline of said first subarray with a said bitline and a complementary said bitline of said second subarray in response to a received control signal,” as recited in claim 11. Nor does Patent Owner dispute that circuitry is required to generate these signals. Rather, Patent Owner argues that the claimed column control circuitry of claim 7 is “***required to be in the alleged memory subsystem of Konishi,***” and that the ϕ BA and ϕ TDS signals could be generated outside of Figures 5 and 6 of Konishi, which Patent Owner contends is the outer limits of a “memory subsystem.” PO Resp. 49–50; *see also id.* at 53–54 (same argument for the control circuitry of claim 11). According to Patent Owner, Petitioner has not shown that Konishi’s memory subsystem necessarily, or inherently, includes column control circuitry because Mr. Murphy’s declaration does not evidence that “‘column control circuitry’ is necessarily within the ‘memory subsystem’ defined by Toshiba—i.e., necessarily within the dotted lines of annotated FIGs. 5 and 6.” *Id.* at 50 (emphasis omitted) (depicting Figures 5 and 6, each annotated with a dotted line encircling the figure); *see also id.* at 54–55 (making substantially the same arguments for claim 11).

We are not persuaded by Patent Owner’s arguments. Patent Owner has not explained persuasively why a “memory subsystem” is limited to the structure depicted in Konishi’s Figures 5 and 6. Patent Owner argues that it would have been possible to generate the ϕ BA and ϕ TDS signals “off-chip (e.g., outside the memory subsystems of FIGs. 5 and 6 of Konishi).” PO Resp. 52. Nevertheless, Patent Owner does not explain persuasively why a memory subsystem is limited to a single chip such that the control circuitry recited in claims 7 and 11 must be included on the same chip as the

memory cells. Indeed, as explained above, the '132 patent explicitly states that “the present invention is not limited to single chip embodiments.”

Ex. 1001, 7:8–9.³

We are persuaded by Petitioner’s evidence that the ϕ BA and ϕ TDS signals perform the functions recited in claims 7 and 11. We further are persuaded that circuitry necessarily is required to generate Konishi’s ϕ BA and ϕ TDS signals. As described in the '132 patent, the recited control circuitry can be included on the same chip as the memory cells or on separate chips. Accordingly, on the full record, Petitioner has shown by a preponderance of the evidence that Konishi anticipates claims 7 and 11.

5. Claims 28 and 29

Regarding claim 28, Petitioner argues that Konishi describes a method for performing a data transfer in a memory subsystem, identifying the same evidence it cited for the memory subsystem of claim 6. Pet. 25–26.

Petitioner further argues that:

Konishi’s row decoder 14 carrying out a row selecting operation in the DRAM array is “activating a selected wordline in the first subarray,” as recited in claim 28;

Konishi’s sense amplifiers differentially amplifying the potential difference between each bitline pair of the DRAM array

³ As explained above, Patent Owner argued at the hearing that this portion of the Specification should be read as describing that “you would separate control circuitry for memory and put that on a chip and you keep that -- the arrays together on a different chip. That’s the multichip embodiment.” Tr. 43:23–44:6. Patent Owner does not reconcile this argument with its position that the control circuitry of claims 7 and 11 must be included on the same chip as the memory.

(Ex. 1004, 14:43–57) is “sensing data at the bitlines of the first subarray from the cells of the selected row”;

activating Konishi’s gates CSG, IOGa, IOGb, BTGa, and BTGb to couple the data from the bitlines DBL of the DRAM array to the bitlines SBL of the SRAM array is “activating a selected group of the gates to couple the sensed data from ones of the bitlines of the first subarray to selected ones of the bitlines of the second subarray”; and

Konishi’s row decoder 21 carrying out a row selecting operation in the SRAM array is “activating a selected wordline of the second subarray to write data from the first subarray into cells of a selected row and the columns associated with the selected bitlines of the second subarray.”

Pet. 26–28.

Patent Owner argues that Konishi does not disclose memory cell partitions in which the partitions have the same type of memory cells as one another and, thus, does not disclose the “first subarray” and “second subarray” of claim 28. PO Resp. 42–43. As explained in Section II.A.1 above, however, “a first subarray” and “a second subarray,” as recited in claim 28, are not limited to partitions with the same type of memory cells. Thus, Patent Owner’s argument is not persuasive.

Patent Owner also argues that Konishi does not disclose “a memory subsystem,” as recited in claim 28, because it discloses transferring data between memories having different types of memory cells. PO Resp. 35–38, 41–42. As explained in Sections II.A.1 and II.A.2, above, however, “a memory subsystem,” as recited in claim 28, is not limited to a single memory with the same type of memory cells. Patent Owner does not otherwise dispute Petitioner’s description of the disclosure of Konishi. Tr. 54:3–6.

We have considered the evidence presented by Petitioner and Patent Owner. On the full record, Petitioner has shown by a preponderance of the evidence that Konishi anticipates claim 28.

We also have considered Petitioner's evidence and argument for claim 29, which depends from claim 28. Pet. 28. Patent Owner does not argue claim 29 separately. PO Resp. 43. On the full record, Petitioner has shown by a preponderance of the evidence that Konishi anticipates claim 29.

C. Anticipation by Fujishima

Petitioner contends that Fujishima anticipates claims 1–12, 28, and 29 of the '132 patent. Petitioner supports its contentions with the testimony of Mr. Murphy (Ex. 1008).

1. Overview of Fujishima

Fujishima describes a semiconductor memory device with a DRAM memory cell array and an SRAM memory cell array. Ex. 1005, Abstract. The SRAM array acts as a cache memory. *Id.* At the time of a cache hit, the SRAM array is accessed; at the time of a cache miss, the DRAM array is accessed and data from a row of the DRAM array are transferred to a row in a corresponding block of the SRAM array. *Id.* Figure 6, reproduced below, illustrates an example:

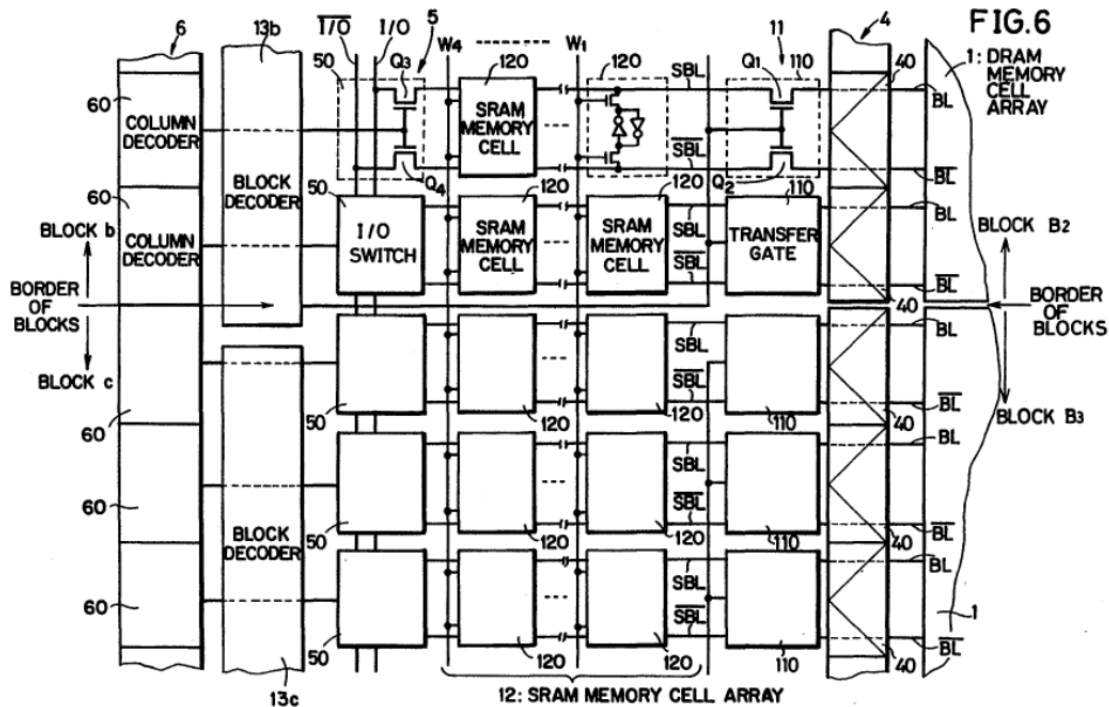


Figure 6 is a block diagram showing the structure of part of a DRAM memory device with an SRAM cache. *Id.* at 6:52–54. The DRAM cells are arranged in blocks B1–B4 (shown in Figure 5). *Id.* at 7:16–18. The SRAM cells are arranged in blocks a–d corresponding to the blocks B1–B4 of the DRAM array. *Id.* at 7:24–27. Bitline pairs BL, \overline{BL} of DRAM memory cell array 1 are coupled to bitline pairs SBL, \overline{SBL} of SRAM memory cell array 12 through sense amplifiers 40 and MOSFETs Q1, Q2 of transfer gates 110. *Id.* at 7:45–68. Block decoders 13a–13d (corresponding to DRAM blocks B1–B4 and SRAM blocks a–d) apply transfer signals to MOSFETs Q1, Q2 of the corresponding transfer gates 110 to transfer data from one row in a block of the DRAM array to a corresponding block of the SRAM array. *Id.* at 7:22–23, 8:5–20.

2. *Claims 1–5*

Regarding claim 1, Petitioner contends that:

Fujishima's DRAM array 1 and bitline pairs BL, $\overline{\text{BL}}$, together, are the recited "first plurality of columns of memory cells each including at least one conductive bitline;"

Fujishima's SRAM array 12 and bitline pairs SBL, $\overline{\text{SBL}}$, together, are the recited "second plurality of columns of memory cells each including at least one conductive bitline;" and

Fujishima's transfer gates 110 are gates organized in groups for selectively coupling the bitlines BL, $\overline{\text{BL}}$ of a selected group of the DRAM cells with a group of the bitlines SBL, $\overline{\text{SBL}}$ of the SRAM array for transferring at least one bit of data from a selected cell of the DRAM array to a selected cell of the SRAM array.

Pet. 30–32. According to Petitioner, each block decoder independently controls a group of transfer gates 110 corresponding to one of the DRAM blocks B1–B4. Pet. 31–32. Thus, Petitioner argues, the plurality of gates is organized in independently controlled groups. *Id.*

Patent Owner argues that Fujishima does not anticipate claim 1 because it discloses transferring data between memories having different types of memory cells. PO Resp. 35–38, 45–46. As explained in Sections II.A.1 and II.A.2, above, however, "a memory," as recited in claim 1, is not limited to a single memory with the same type of memory cells.

Accordingly Patent Owner's argument is not persuasive. Rather, we find that Fujishima's DRAM and SRAM, together, constitute "one or more memories," as we have construed "a memory." Patent Owner does not otherwise dispute Petitioner's description of the disclosure of Fujishima. Tr. 54:3–6 ("[T]here is no dispute between the parties relative to how . . .

Fujishima operate[s]. The parties agree regarding the technical operation[] of Fujishima.”).

We have considered the evidence presented by Petitioner and Patent Owner. On the full record, Petitioner has shown by a preponderance of the evidence that Fujishima anticipates claim 1.

We also have considered Petitioner’s evidence and argument for claims 2, 3, and 5. For example, regarding claim 5, Petitioner contends that Fujishima discloses that the DRAM array includes a plurality of rows of cells and that each row includes a conductive wordline WL that is controlled by a row decoder portion 3 (shown in Figure 5 of Fujishima). Pet. 33. Likewise, Petitioner argues that the SRAM array includes a plurality of rows of cells, that each row includes a conductive wordline W1–W4, and that each wordline is controlled by a way decoder 14 (shown in Figure 5). *Id.* Patent Owner does not argue claims 2, 3, and 5 separately. PO Resp. 48. On the full record, Petitioner has shown by a preponderance of the evidence that Fujishima anticipates claims 2, 3, and 5.

Claim 4 recites “a first subarray” and “a second subarray.” Patent Owner argues that Fujishima does not disclose memory cell partitions in which the partitions have the same type of memory cells as one another and, thus, does not anticipate claim 4. PO Resp. 46–48. As explained in Section II.A.1 above, however, “a first subarray” and “a second subarray” as recited in claim 4, are not limited to partitions with the same type of memory cells. Thus, Patent Owner’s argument is not persuasive.

We find that Fujishima’s DRAM array is “a first memory cells partition including a plurality of rows and columns of memory cells” and that Fujishima’s SRAM array is “a second memory cells partition including

a plurality of rows and columns of memory cells.” We have considered the evidence presented by Petitioner and Patent Owner. On the full record, Petitioner has shown by a preponderance of the evidence that Fujishima anticipates claim 4.

3. Claims 6–12

Petitioner relies on the embodiment shown in Fujishima’s Figures 9 and 10 as showing the features of claim 6. Pet. 33–35. This embodiment includes many of the features of the embodiment illustrated in Figure 6, reproduced above, along with modifications. Ex. 1005, 12:18–24.

Specifically, Petitioner contends that:

Fujishima’s DRAM array, along with its associated bitline pairs and wordlines, is a first subarray;

Fujishima’s SRAM array, along with its associated bitline pairs and wordlines, is a second subarray;

Fujishima’s block transfer gate portion 11 and additional way transfer gates 42 are circuitry for independently coupling selected groups of the bitlines of the DRAM subarray with corresponding groups of the bitlines of the SRAM subarray; and

Fujishima’s normal column decoder 6 and cache column decoder portion 45 (shown in Figure 9) are first and second column decoders, respectively.

Pet. 33–35.

Patent Owner argues that Fujishima does not disclose memory cell partitions in which the partitions have the same type of memory cells as one another and, thus, does not disclose the “first subarray” and “second subarray” of claim 6. PO Resp. 46–48. As explained in Section II.A.1

above, however, “a first subarray” and “a second subarray” as recited in claim 6, are not limited to partitions with the same type of memory cells. Thus, Patent Owner’s argument is not persuasive.

Patent Owner also argues that Fujishima does not disclose “a memory subsystem,” as recited in claim 6, because it discloses transferring data between memories having different types of memory cells. PO Resp. 35–38, 45–46. As explained in Sections II.A.1 and II.A.2, above, however, “a memory subsystem,” as recited in claim 6, is not limited to a single memory with the same type of memory cells. Patent Owner does not otherwise dispute Petitioner’s description of the disclosure of Fujishima. Tr. 54:3–6.

We have considered the evidence presented by Petitioner and Patent Owner. On the full record, Petitioner has shown by a preponderance of the evidence that Fujishima anticipates claim 6.

We also have considered Petitioner’s evidence and argument for claims 7–12. Pet. 35–36. For example, regarding claim 8, Petitioner argues that Fujishima’s DRAM bitline pairs BL_1 – BL_n and SBL_1 – SBL_m (shown in Figure 10) are complementary pairs and, thus, pairs of folded bitlines. Pet. 35. As shown in Fujishima’s Figure 10, bitline pairs BL_1 – BL_n and SBL_1 – SBL_m are generally parallel to one another. Thus, we are persuaded that they are folded bitlines under either party’s proposed construction. Patent Owner does not argue claims 7–12 separately. PO Resp. 48. On the full record, Petitioner has shown by a preponderance of the evidence that Fujishima anticipates claims 7–12.

4. Claims 28 and 29

Regarding claim 28, Petitioner argues that Fujishima describes a method for performing a data transfer in a memory subsystem, identifying the same evidence it cited for the memory subsystem of claim 6. Petition 36–37. Petitioner further argues that:

- Fujishima’s row decoder portion 3 selecting a word line WL is activating a selected wordline in the first (DRAM) subarray;
- Fujishima’s sense amplifiers 40 of sense amplifier portion 4 (shown in Figure 6, reproduced above) sensing data at bitlines BL, \overline{BL} is sensing data at the bitlines of the first subarray from the cells of a selected row;
- activating groups of transfer gates 110 to couple the sensed data from the bitlines BL, \overline{BL} of the DRAM array to the bitlines SBL, \overline{SBL} of the SRAM array, as disclosed in Fujishima, is activating a selected group of the gates to couple sensed data from ones of the bitlines of the first subarray to selected ones of the bitlines of the second subarray; and
- activating a selected wordline W_1 – W_4 of SRAM array 12 (shown in Figure 10 of Fujishima) to write data from the DRAM array into selected rows and columns associated with selected bitlines SBL, \overline{SBL} of the SRAM array is activating a selected wordline of the second subarray to write the data from the first subarray into cells of a selected row and the columns associated with the selected bitlines of the second subarray.

Pet. 37–38.

Patent Owner argues that Fujishima does not disclose memory cell partitions in which the partitions have the same type of memory cells as one another and, thus, does not disclose the “first subarray” and “second subarray” of claim 28. PO Resp. 46–48. As explained in Section II.A.1 above, however, “a first subarray” and “a second subarray,” as recited in

claim 28, are not limited to partitions with the same type of memory cells. Thus, Patent Owner's argument is not persuasive.

Patent Owner also argues that Fujishima does not disclose "a memory subsystem," as recited in claim 28, because it discloses transferring data between memories having different types of memory cells. PO Resp. 35–38, 45–46. As explained in Sections II.A.1 and II.A.2, above, however, "a memory subsystem," as recited in claim 28, is not limited to a single memory with the same type of memory cells. Patent Owner does not otherwise dispute Petitioner's description of the disclosure of Fujishima. Tr. 54:3–6.

We have considered the evidence presented by Petitioner and Patent Owner. On the full record, Petitioner has shown by a preponderance of the evidence that Fujishima anticipates claim 28.

We also have considered Petitioner's evidence and argument for claim 29, which depends from claim 28. Pet. 28. Patent Owner does not argue claim 29 separately. PO Resp. 48. On the full record, Petitioner has shown by a preponderance of the evidence that Fujishima anticipates claim 29.

III. CONCLUSION

Petitioner has demonstrated by a preponderance of the evidence that claims 1–14, 28, and 29 are unpatentable based on the following grounds of unpatentability:

(1) Claims 1–14, 28, and 29 under 35 U.S.C. § 102(e) as anticipated by Konishi; and

(2) Claims 1–12, 28, and 29 under 35 U.S.C. § 102(b) as anticipated by Fujishima.

IV. ORDER

For the reasons given, it is

ORDERED that, based on a preponderance of the evidence, claims 1–14, 28, and 29 of U.S. Patent No. 5,687,132 are held unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to this proceeding seeking judicial review of our Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2014-00317
Patent 5,687,132

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