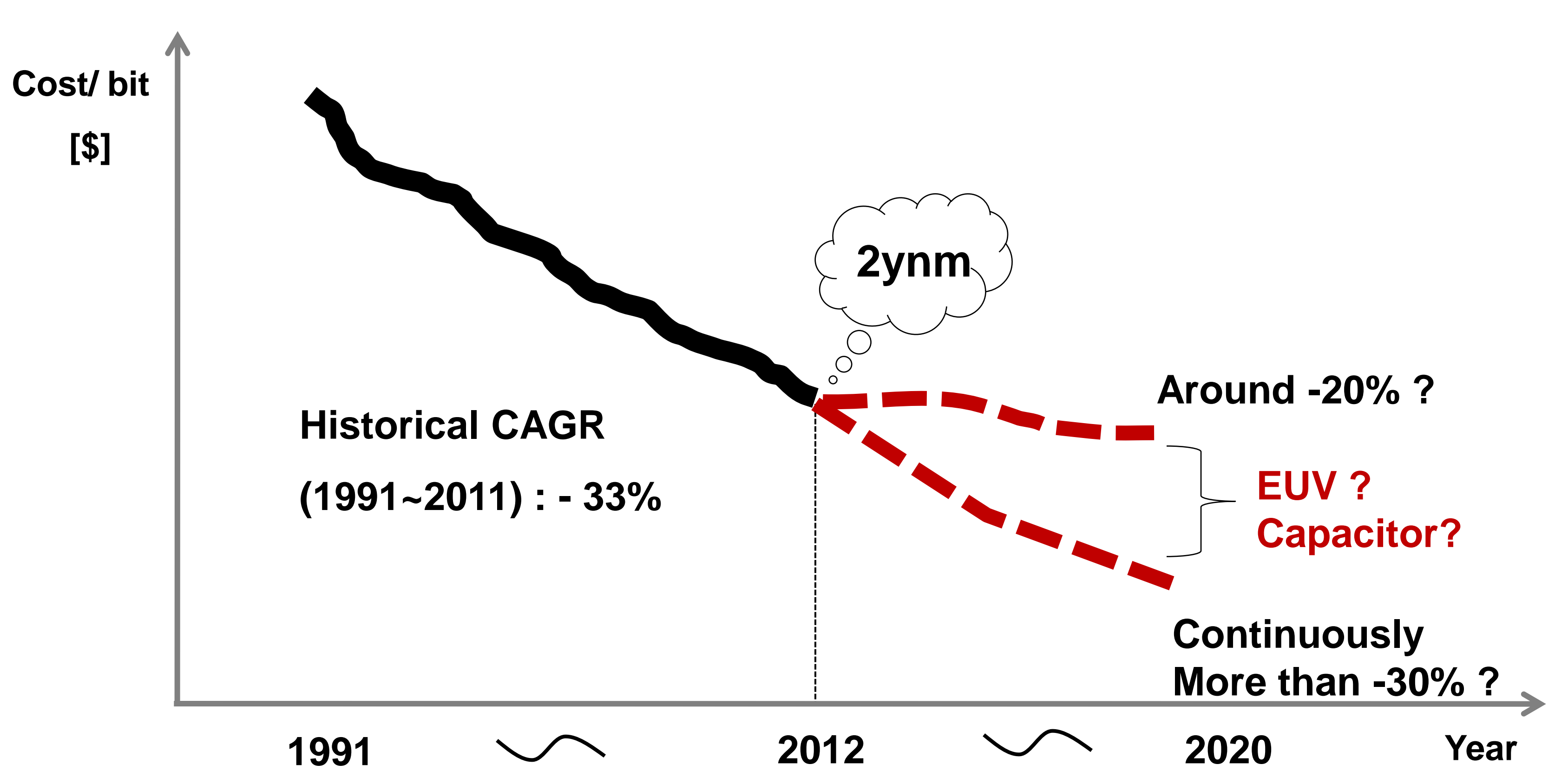
Prospect for New Memory Technology

Sung Wook Park

SK hynix

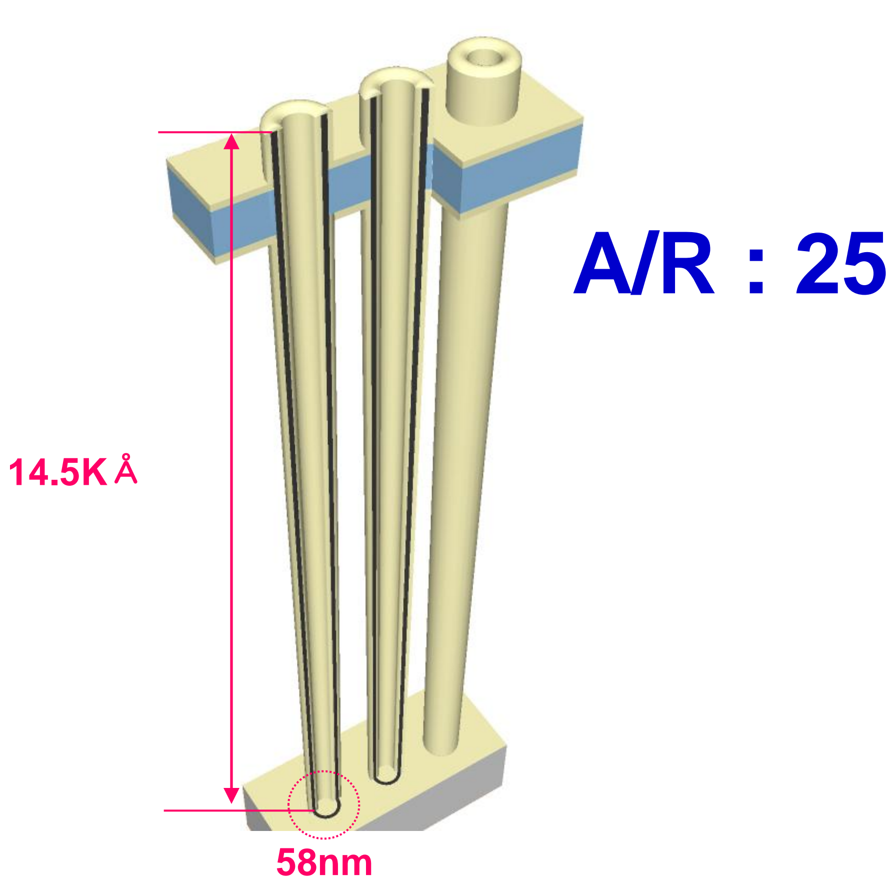
Aug, 2012

DRAM Cost Trend



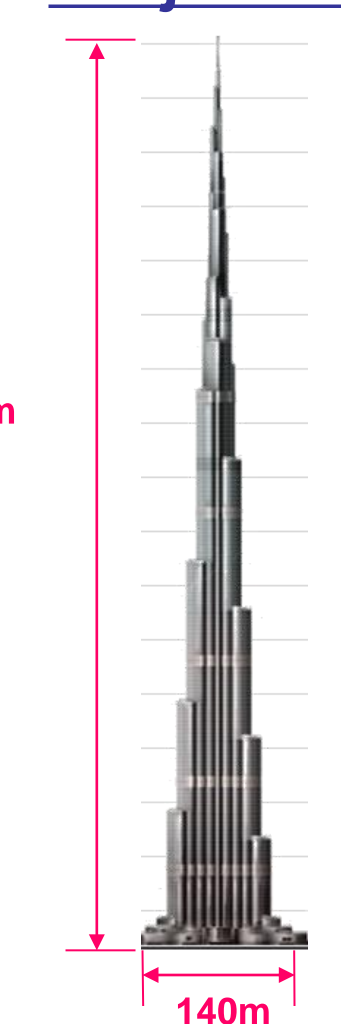
DRAM Challenge : Capacitor

DRAM(3xnm) Capacitor



Burj Khalifa

828m

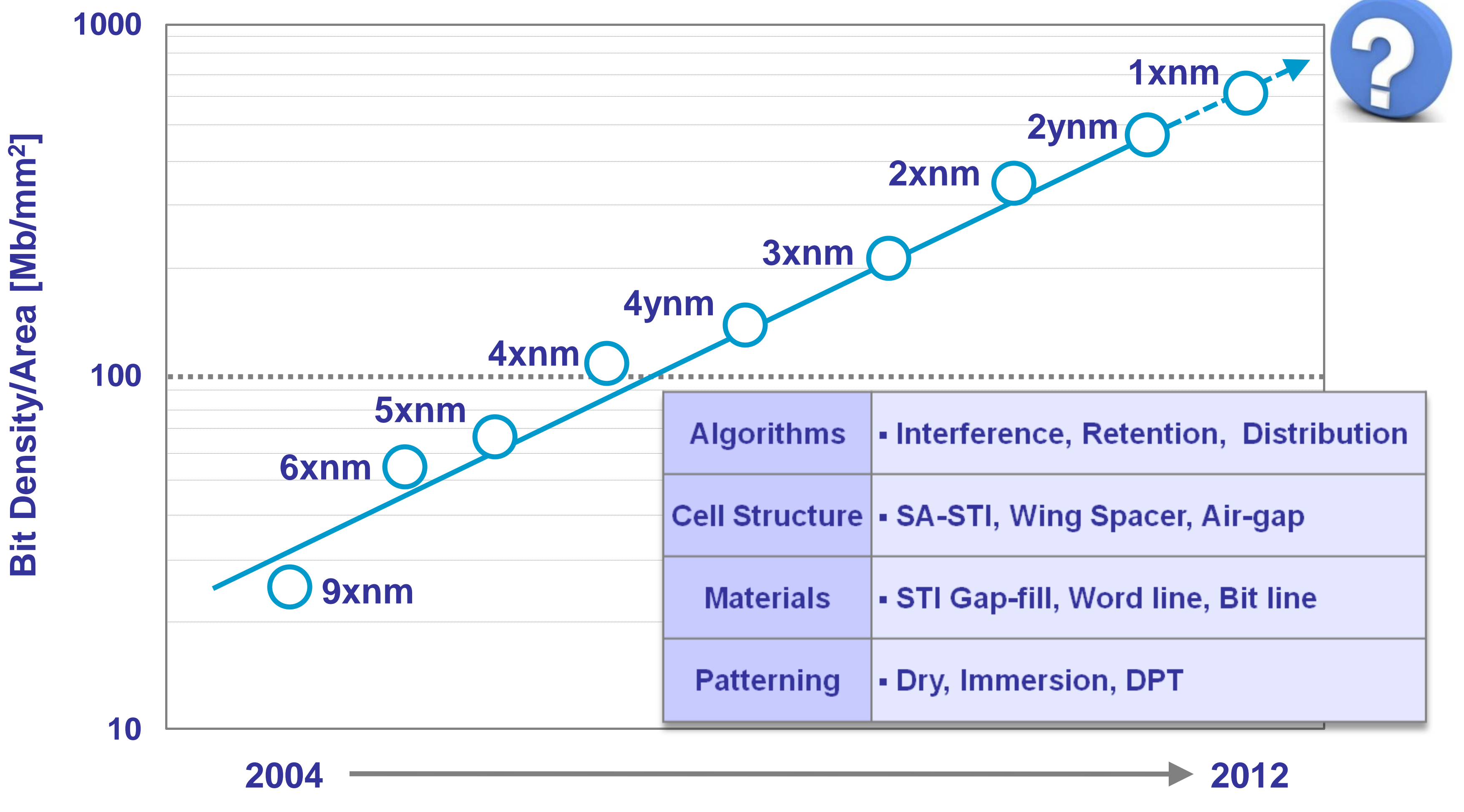


A/R : 6

*) Aspect Ratio : Height / Bottom CD

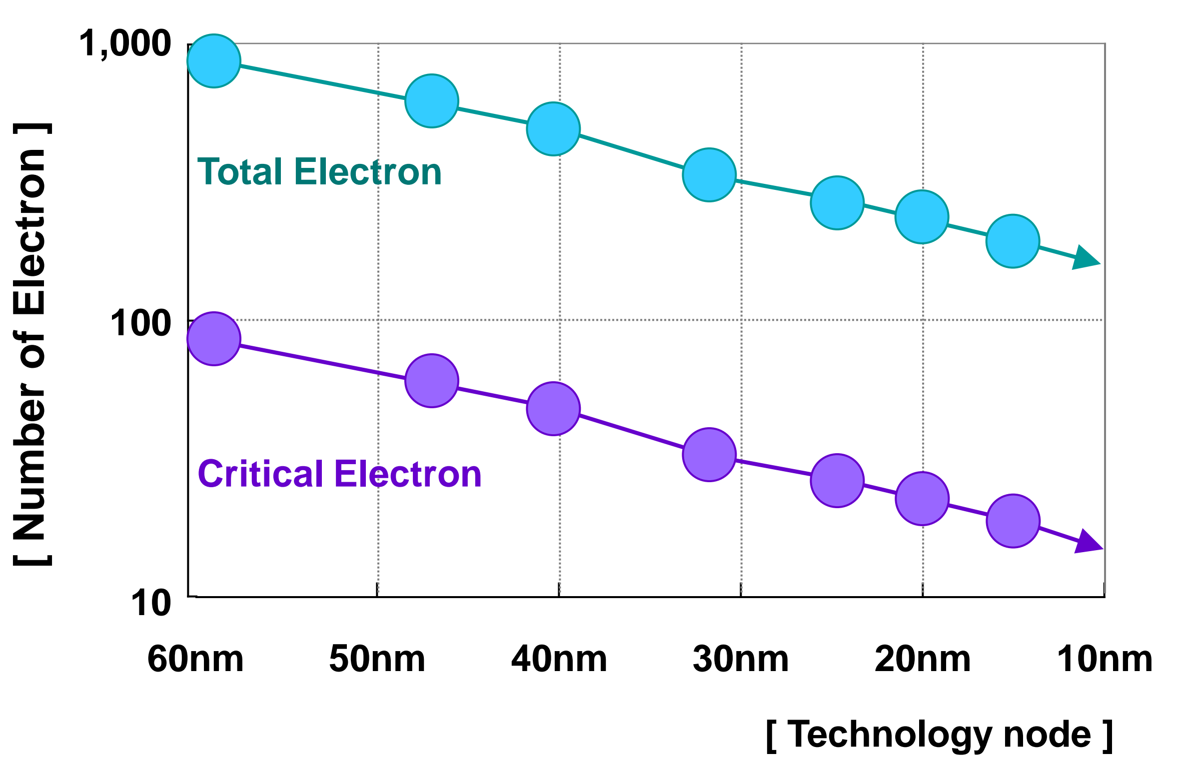
NAND Process Scaling : Lower Cost

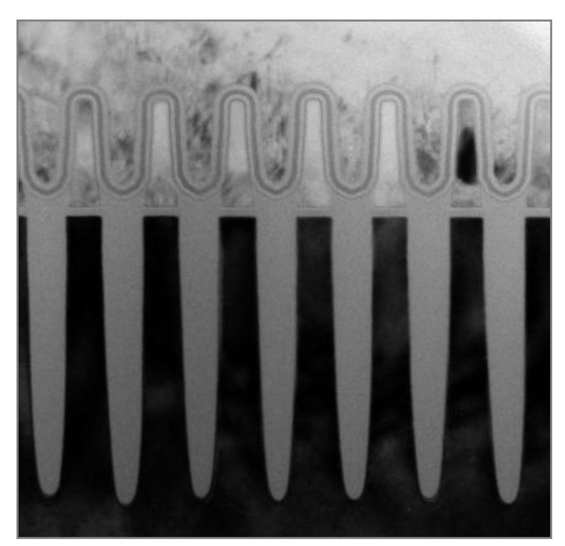
- Increase of bit density/area by ~50% per year
  - One Tech-node per year



Algorithms	▪ Interference, Retention, Distribution
Cell Structure	▪ SA-STI, Wing Spacer, Air-gap
Materials	▪ STI Gap-fill, Word line, Bit line
Patterning	▪ Dry, Immersion, DPT

FG Limitation : Number of Electrons





How to Manage 10 electrons in sub-1xnm design rule?

Key Questions in NAND Scaling

Issues with 10nm FG		Solutions
X - direction	CG poly-Si void	?
	Interference	
	Bit-Line loading	
Y - direction	WL bending	
	Interference	
	WL-to-WL leakage	

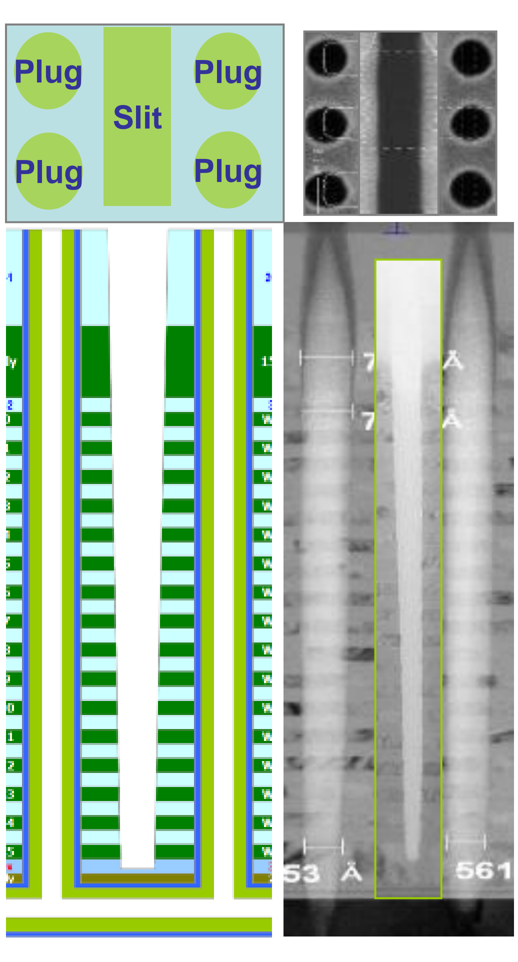
10nm FG?

3D NAND?

Proposed 3D NAND Structure

	p-BiCS (Toshiba)	TCAT (Samsung)	3D FG (Hynix)	Micron
Structure	Bit Line Source Line SG CG PC Slit Tanaka. H, VLSIT 2007	Poly-Si Channel SSL Gate W-Gate Tunnel ox. Control Gate (W/L) Trap SiN Blocking Layer GSL Gate n+ CSL p-Sub J. Jang, VLSIT 2009	CG FG CG S. Whang, IEDM 2010	G. Hawk, FMS 2011
Key Features	- P+ SONOS Cell	- TANOS Cell	- Floating Gate	?
Key Issue	- Large Cell Size - Reliability	- Large Cell Size - SL Resistance	- Process of bit separation - Disturbance	?

3D NAND Challenges : Yield & Retention



- **Factors for Yield**
  - Stabilization of multi-stack patterning
  - Metrology
  - Defect monitoring for deep inside 3D-structure
- **Poor data retention**
  - Needs careful cell optimization

Why New Memory?

Limitations of Conventional Memory Devices

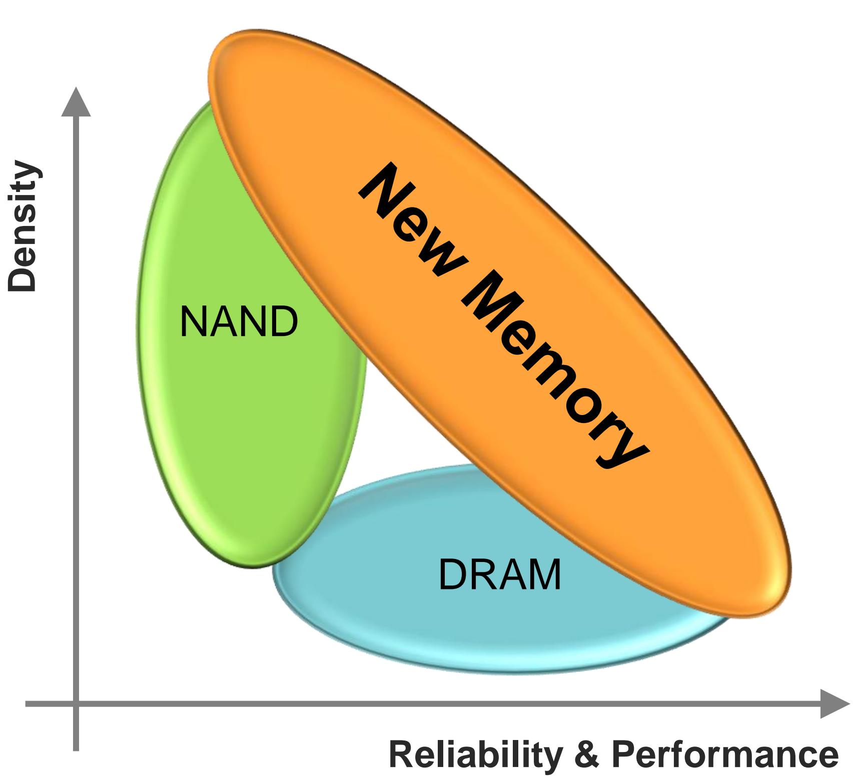
- Cell capacitance below 2xnm?
  - High Density (>8Gb) Challenging

- Electrons in FG below 1xnm?
  - Retention & Reliability degradation
    SLC (< 50k), MLC (<3k)

Solution

New Memory with Improved Scalability & Reliability

New Memory : Potential

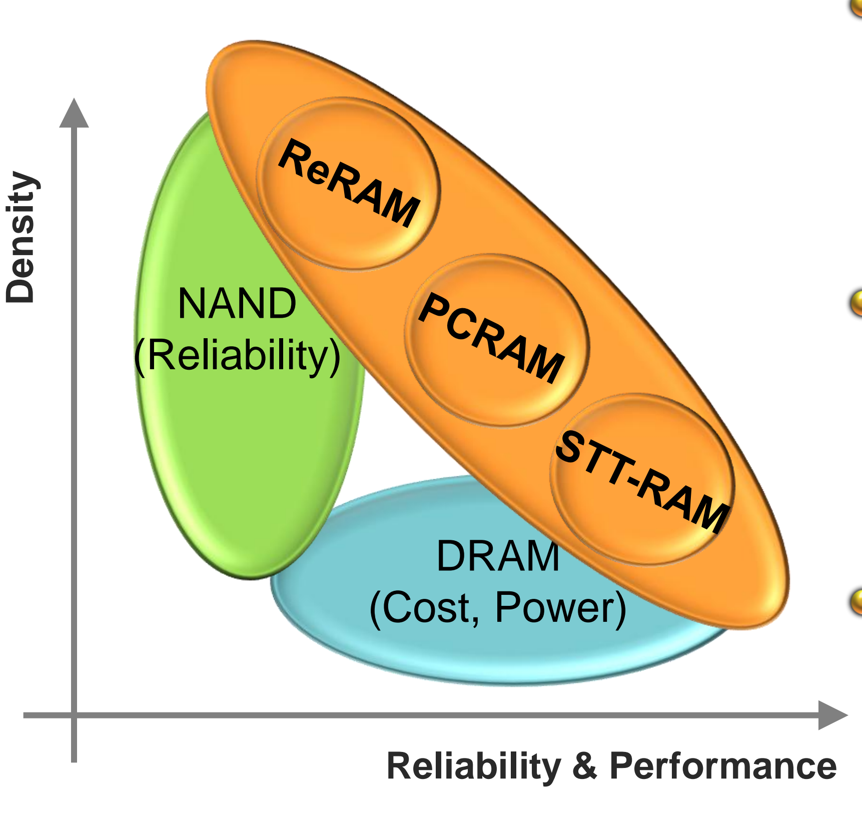


1. **Replace existing memory**
   - Breakthrough on DRAM retention
   - Breakthrough on NAND reliability

2. **Upgrade system performance**
   - Reduce the latency gap
   - Lower power consumption

3. **More scalable solution**
   - Lower cost
   - Smaller form factor

New Memory : Requirements

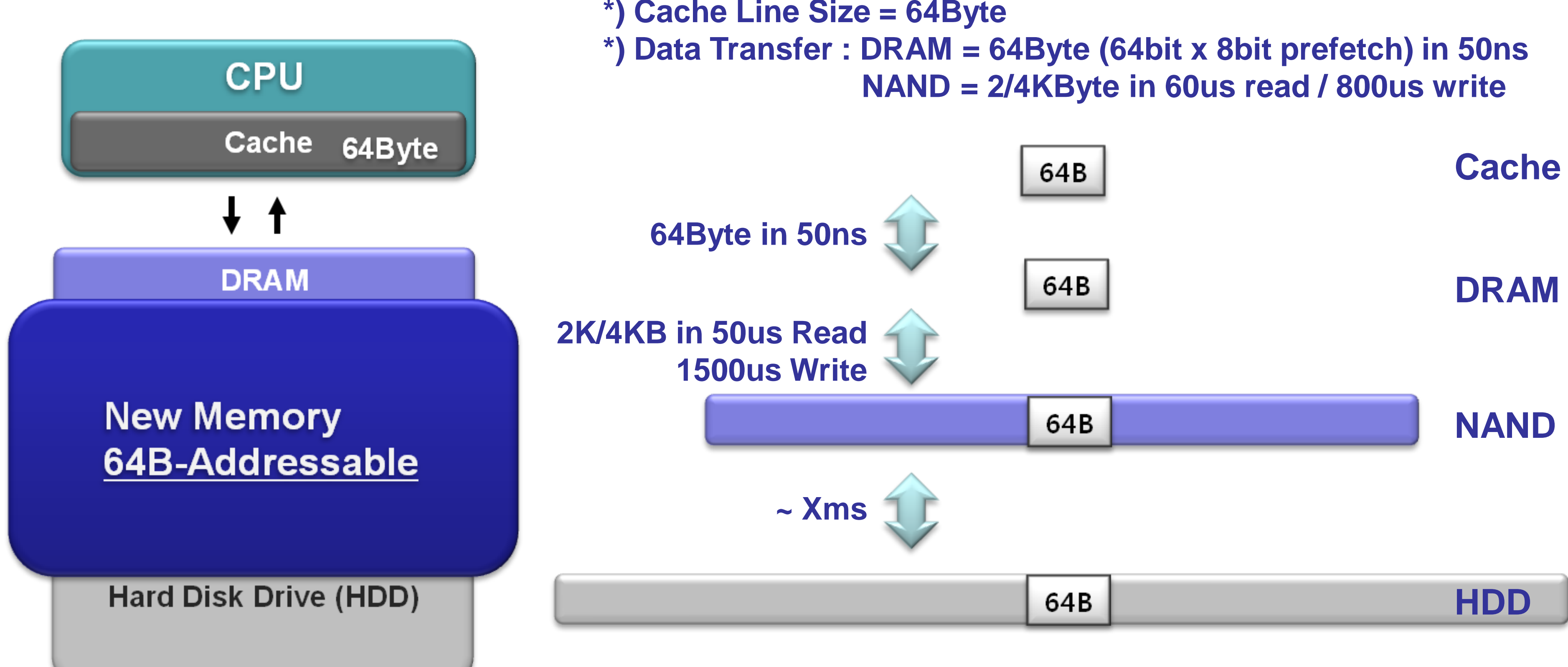


- **Drop in Replacement**
  - Compatible Interface with Conventional Memory (DDRx / LPDDRx)
- **Cost & Power (vs. DRAM)**
  - Cost Down & No Refresh-Power (Scalability & Non-Volatile)
- **Reliability & Performance (vs. NAND)**
  - Implement Native High IOPS (Byte Operation, Better than NAND Reliability)

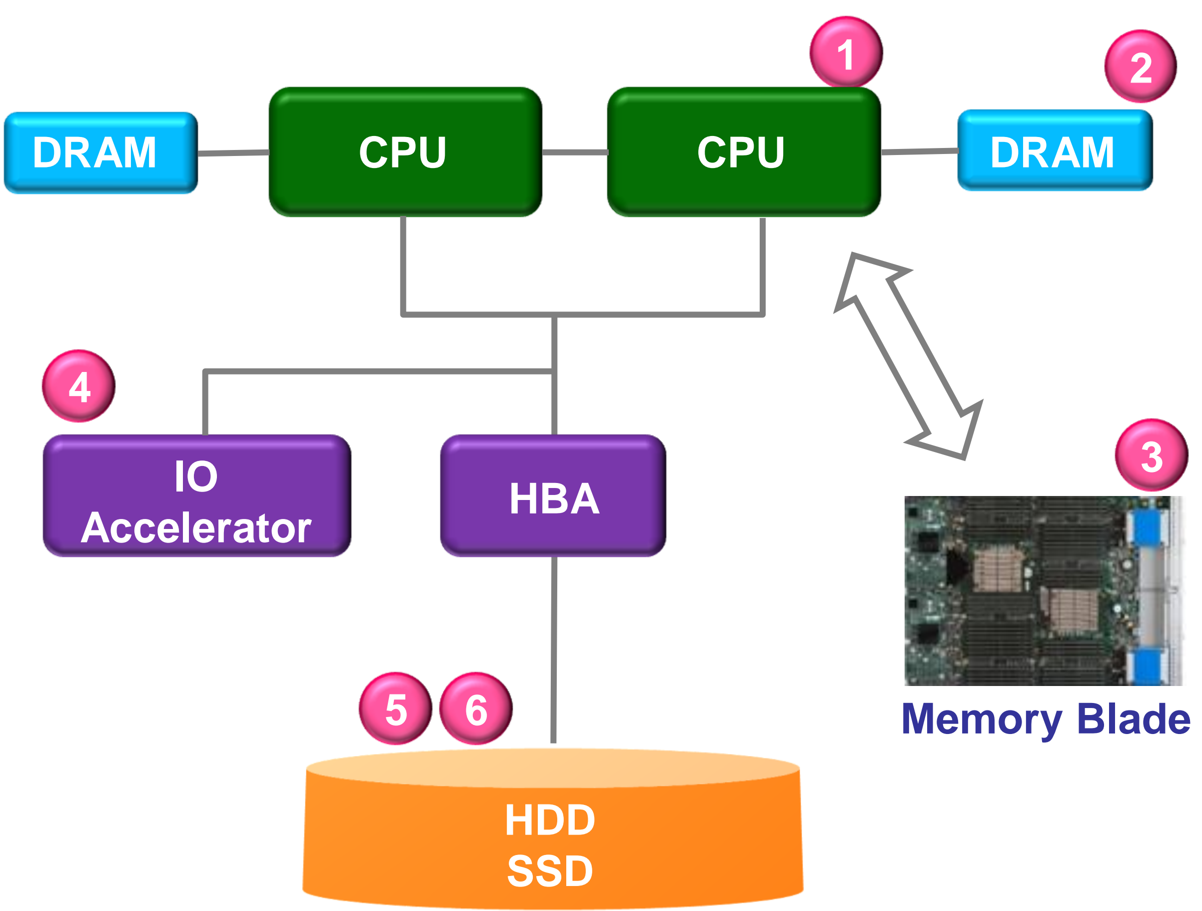
*) New memory technology should meet at least one of requirements

New Memory : High Performance

- DRAM-like Byte Accessability
- Fast & Direct transfer between CPU and High Density Storage

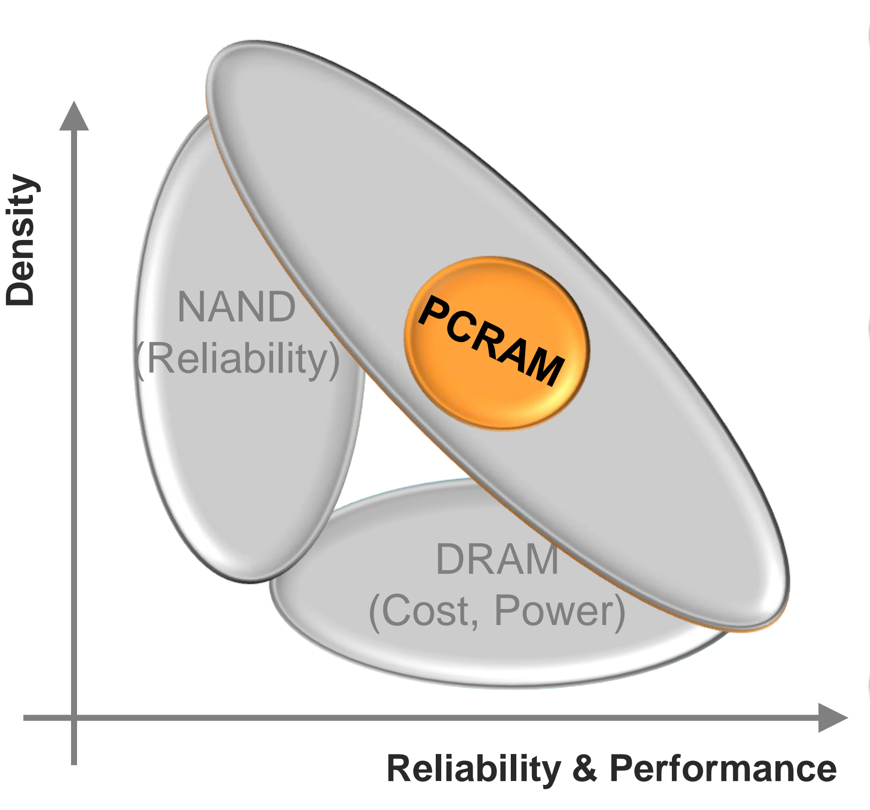


New Memory : Function & Position



1. L3 Cache Extension
   - STT-RAM
2. Working Memory
   - Hybrid STT-RAM & PCRAM
3. Memory Blade
   - PCRAM / ReRAM
4. IO Accelerator
5. SSD
6. HDD
   - PCRAM / ReRAM

PCRAM : Opportunities & Concerns



1. **Advantages of Ge-Sb-Te**
   - Non-volatility / Phase change phenomena
   - Good scalability (< 5nm)

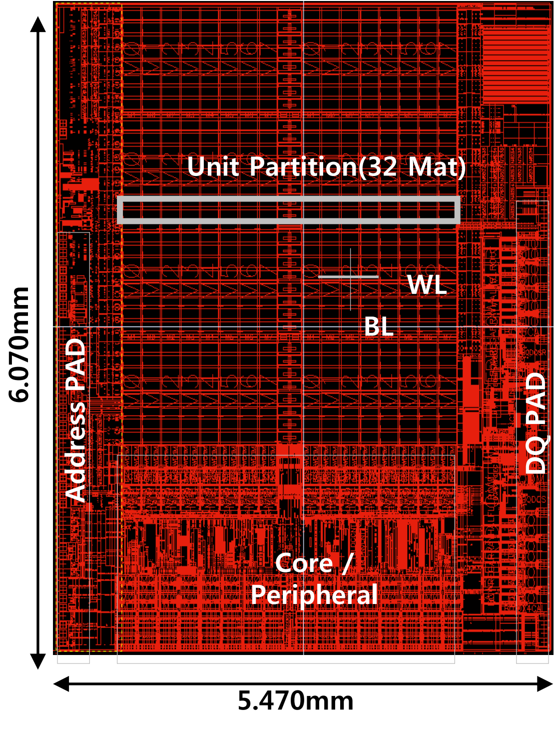
2. **Not replacing but making a new class (Upgrade the system performance)**
   - DRAM-like (Memory-like) : Hybrid
   - NAND-like (Storage-like)

3. **Concerns for DRAM-like application**
   - Cost < 1/2 x DRAM
   - Active power : relatively large reset current

PCRAM : Technology Update

Smaller heater geometry, optimization of heater & GST materials.

1Gb PCRAM, 42nm



<Source : S.H.Lee IEDM 2011>

WL Axis
M1
TML
TML
TE
Confined Cell
BE heater
Poly
Diode
BM
BML
W/L

- 2xnm
- 4F2 Self-aligned structure : Cell + Diode on metal (W/L)

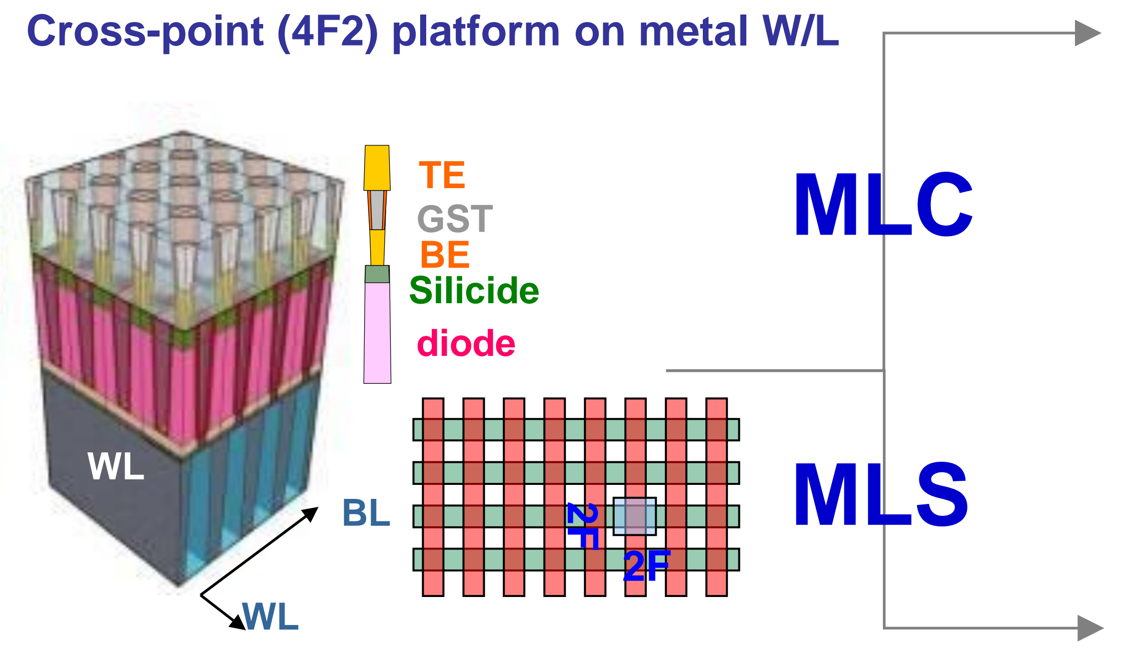
GST: Germanium-Antimony-Tellurium

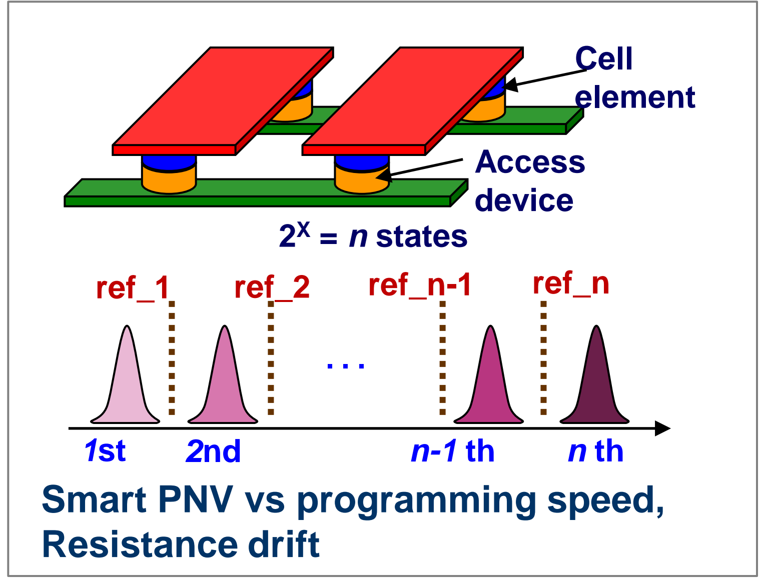
GST
18 nm
64.3 nm
37.9 nm
Diode

PCRAM : Technology Update (2)

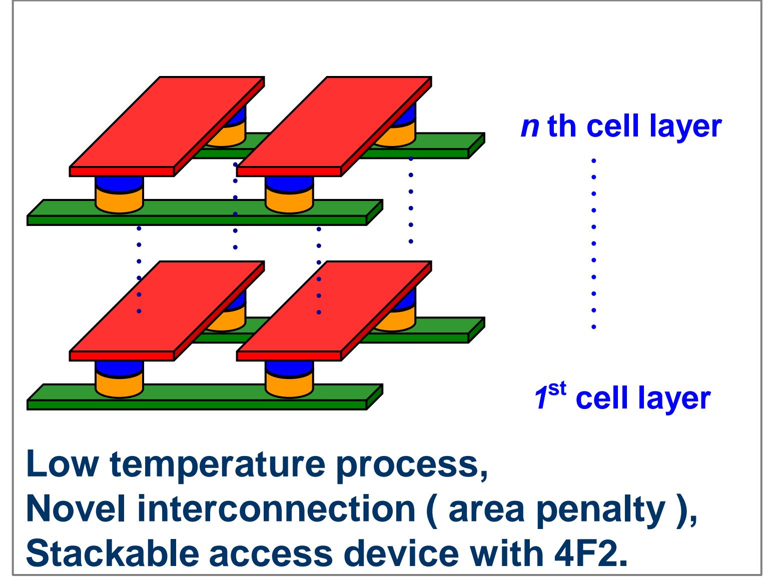
Implement MLC and MLS Technology to enhance Cost Effectiveness

Cross-point (4F2) platform on metal W/L



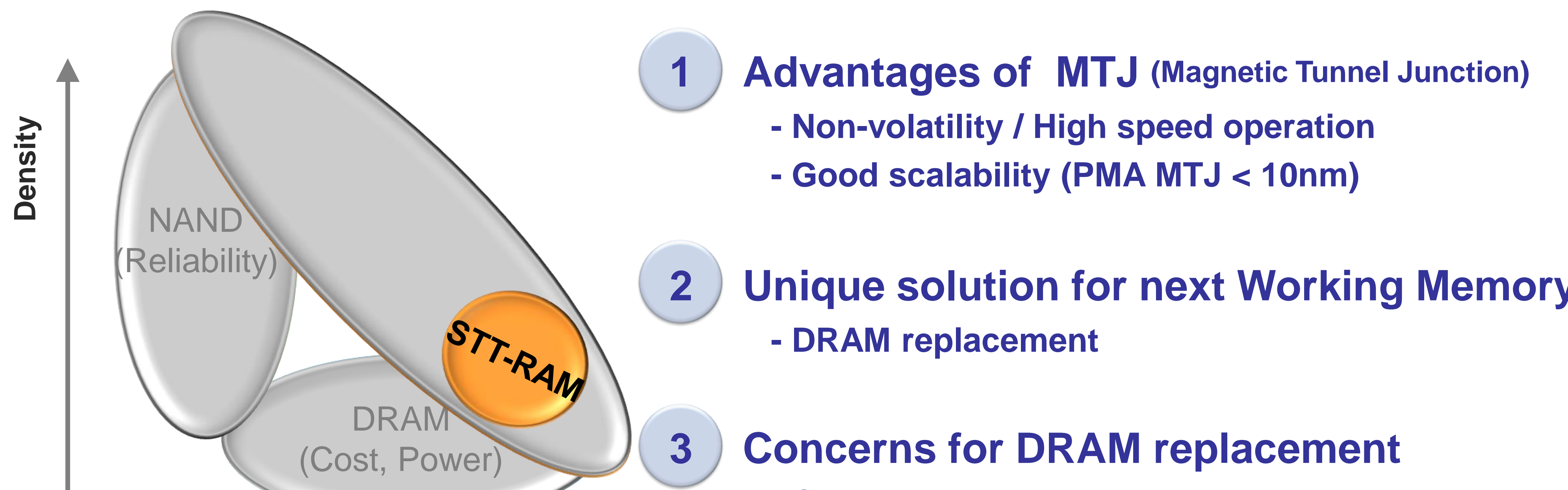


Smart PNV vs programming speed, Resistance drift



Low temperature process,
Novel interconnection (area penalty),
Stackable access device with 4F2.

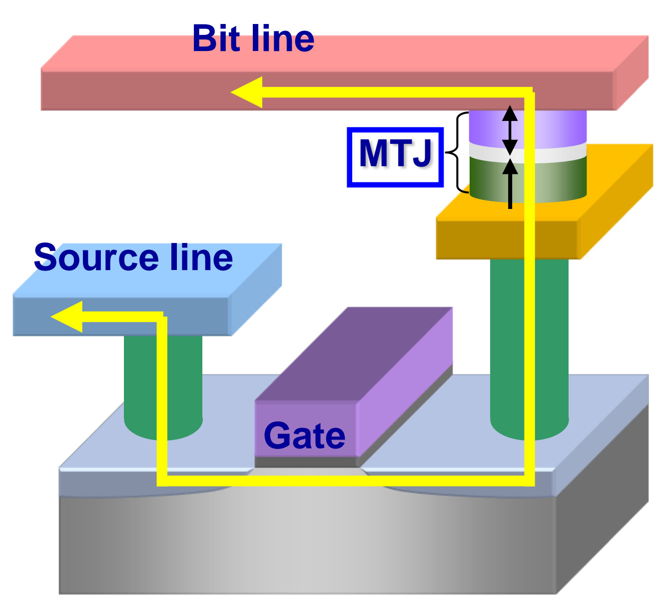
STT-RAM : Opportunities & Concerns

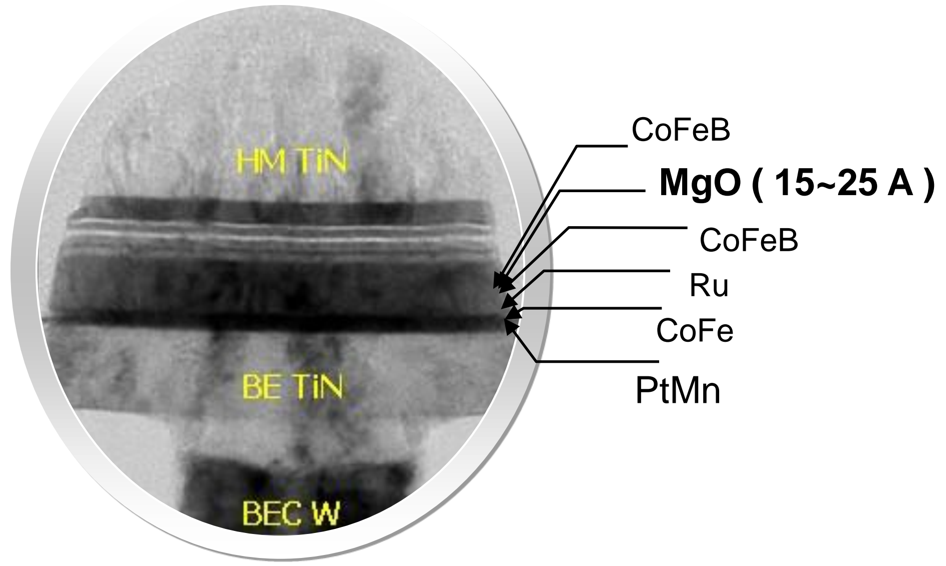


STT-RAM : Technology Update

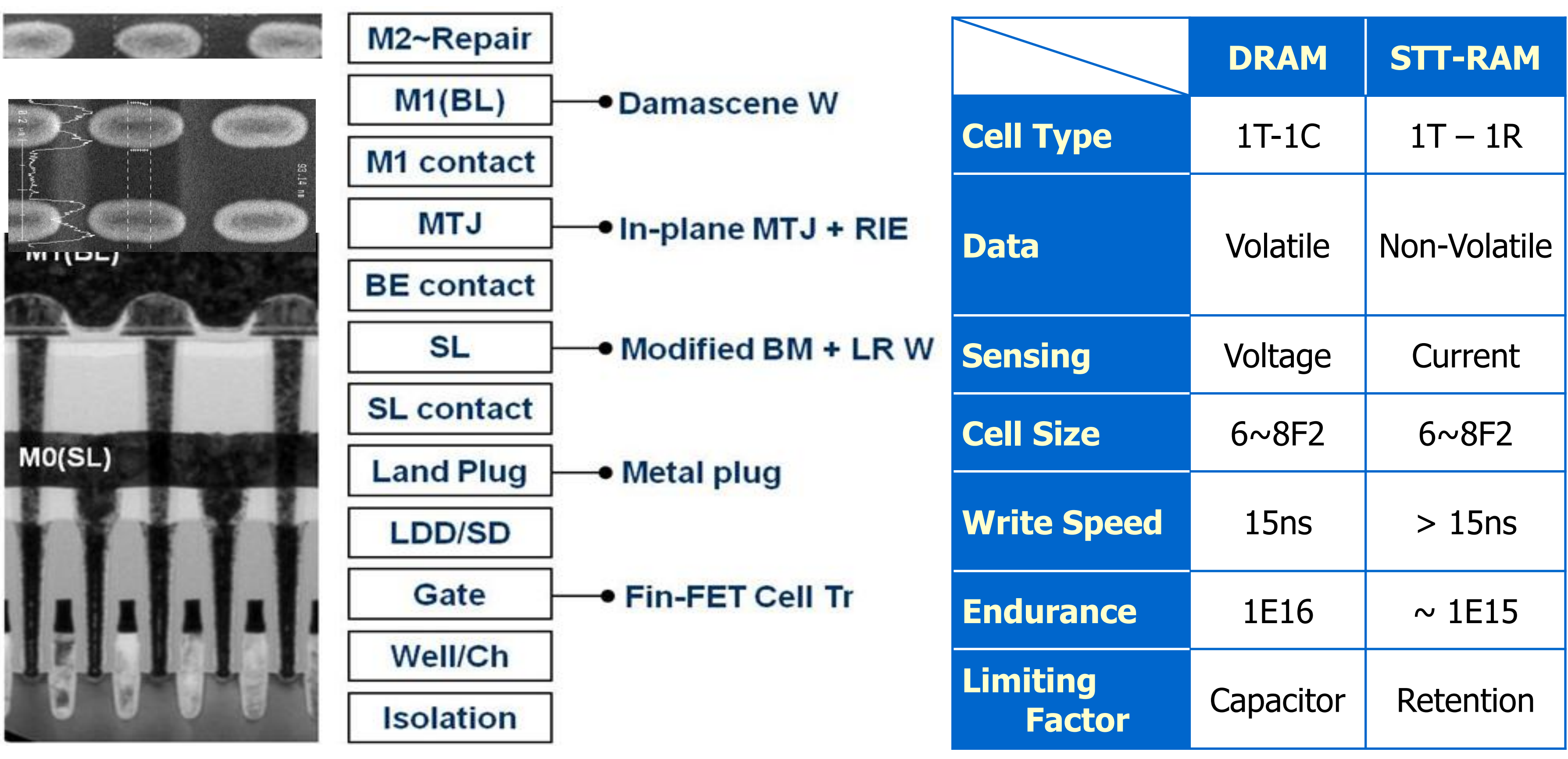
- Low MTJ switching current,
  High thermal stability
  : Perpendicular Magnetic Anisotropy

- Complicated MTJ stacking structure
  : Most critical part.





STT-RAM test chip (IEDM 2010)



	DRAM	STT-RAM
Cell Type	1T-1C	1T – 1R
Data	Volatile	Non-Volatile
Sensing	Voltage	Current
Cell Size	6~8F2	6~8F2
Write Speed	15ns	> 15ns
Endurance	1E16	~ 1E15
Limiting Factor	Capacitor	Retention

- **DRAM friendly cell structure and process integration.**

Technical Challenges

MTJ switching current → major concerning issue
(retention, distribution, read margin)

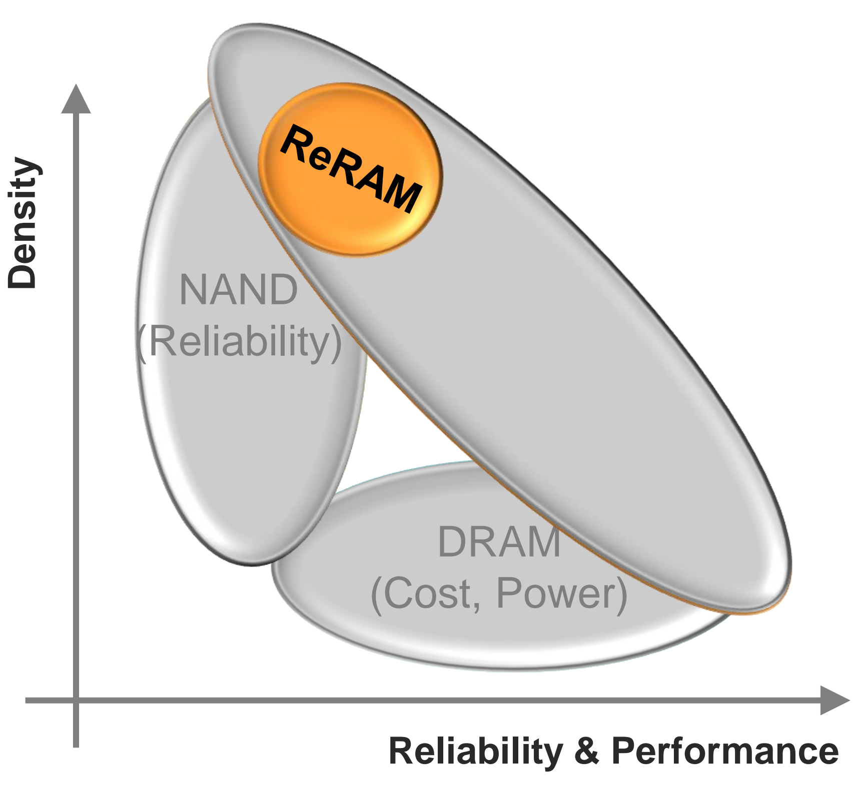
1. MTJ patterning process without degradation of MTJ properties
   - Etching (slope, sidewall damage, shunt…)

2. The reduced total parasitic resistance
   - High performance cell transistor (cell size 14F2 → ?F2)
   - Interconnection resistance (array size limitation)

3. Small data signal (High/Low resistance ratio ~2.5)
   - Required Large Sense amp size
   - Required High TMR (>200%)

4. ECC and Memory controllers

ReRAM : Opportunities & Concerns



1 **Memristor Cell**

- Very simple materials & structure
- Low power operation
  : Non-volatile, Vsw<3V, Isw <10uA

2 **High density storage capability**

- Simple & stackable cell
- NAND or HDD replacement

3 **High performance SCM capability**

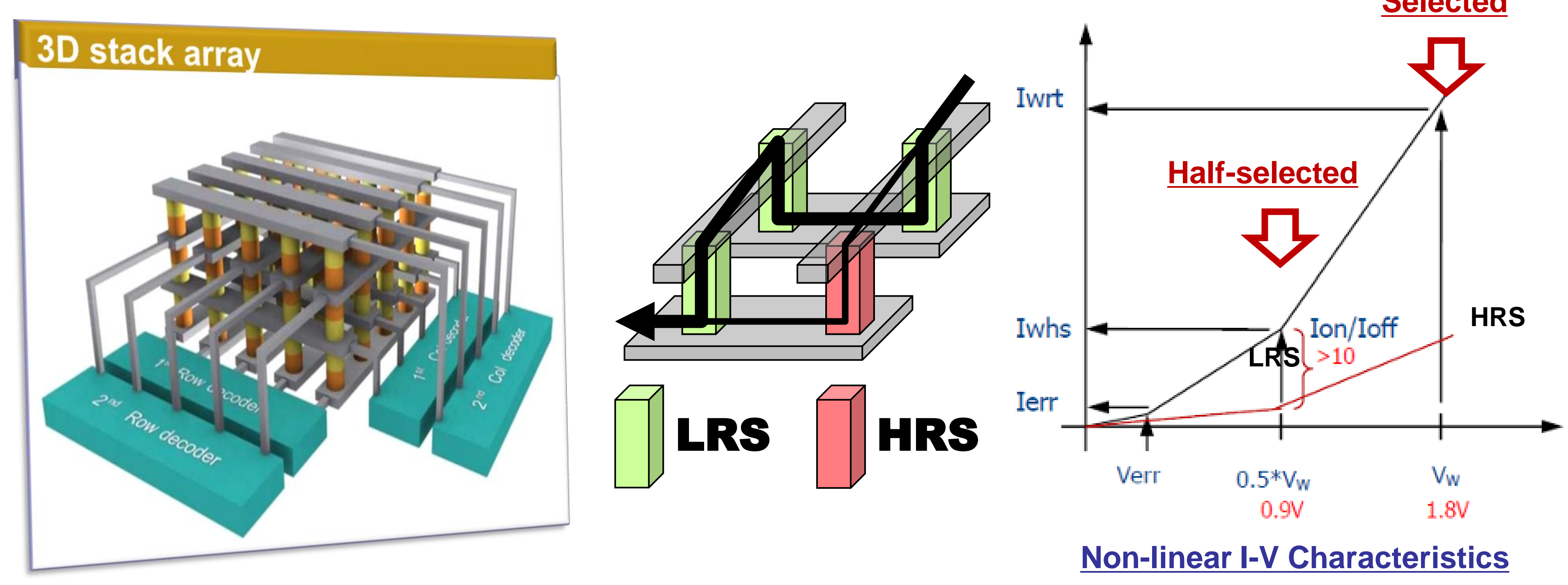
- Fast Access & Good Endurance

4 **Concerns for memory application**

Various & unclear switching mechanism

ReRAM : Technology Update

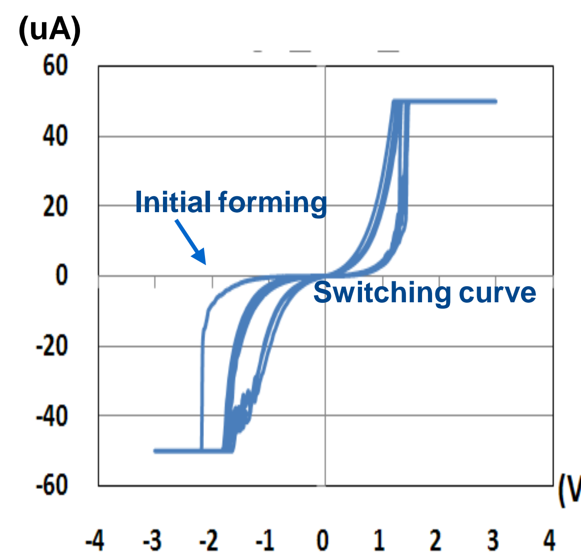
- Maximize the cell array efficiency
  - Multi stack cross bar array architecture
  - Small core overhead : Buried core circuits
- Memristor : Simple cell structure (no switching device)
  - Suppress sneak current : highly non-linear I-V



Non-linear I-V Characteristics

ReRAM : Technology Update (2)

- Memristor cell Technology
  - Simple TMO (Transition metal oxide)
  - Binary switching : symmetric
  - Good non-linear I-V : Kw
  - Low Reset current



VSLI

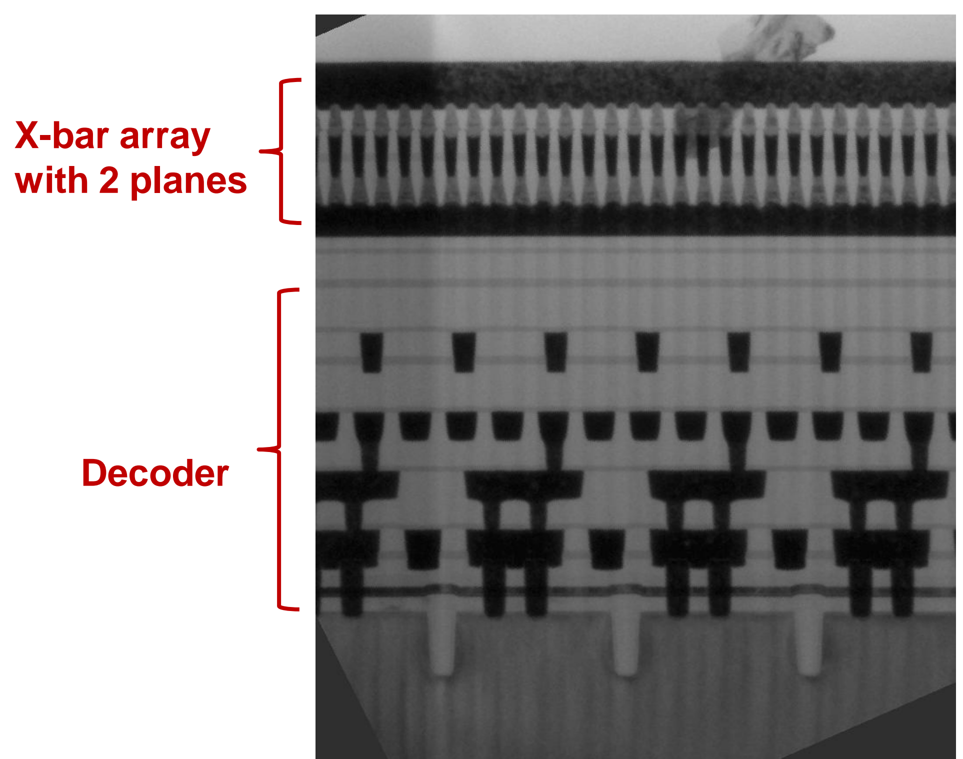
Items	Sample
I_reset (CC)	< 50uA
V_sw_dc	1.6 V
Kw	> 10
on/off	~ 10
V_forming	2.0 V
AC endurance	> 1e4 cycles

ReRAM : Technology Update (3)

- **Multi-planes for high density & cost-efficiency**
  - 8Mb chip design for cross bar array with multi planes
  - Decoders underneath cell array.

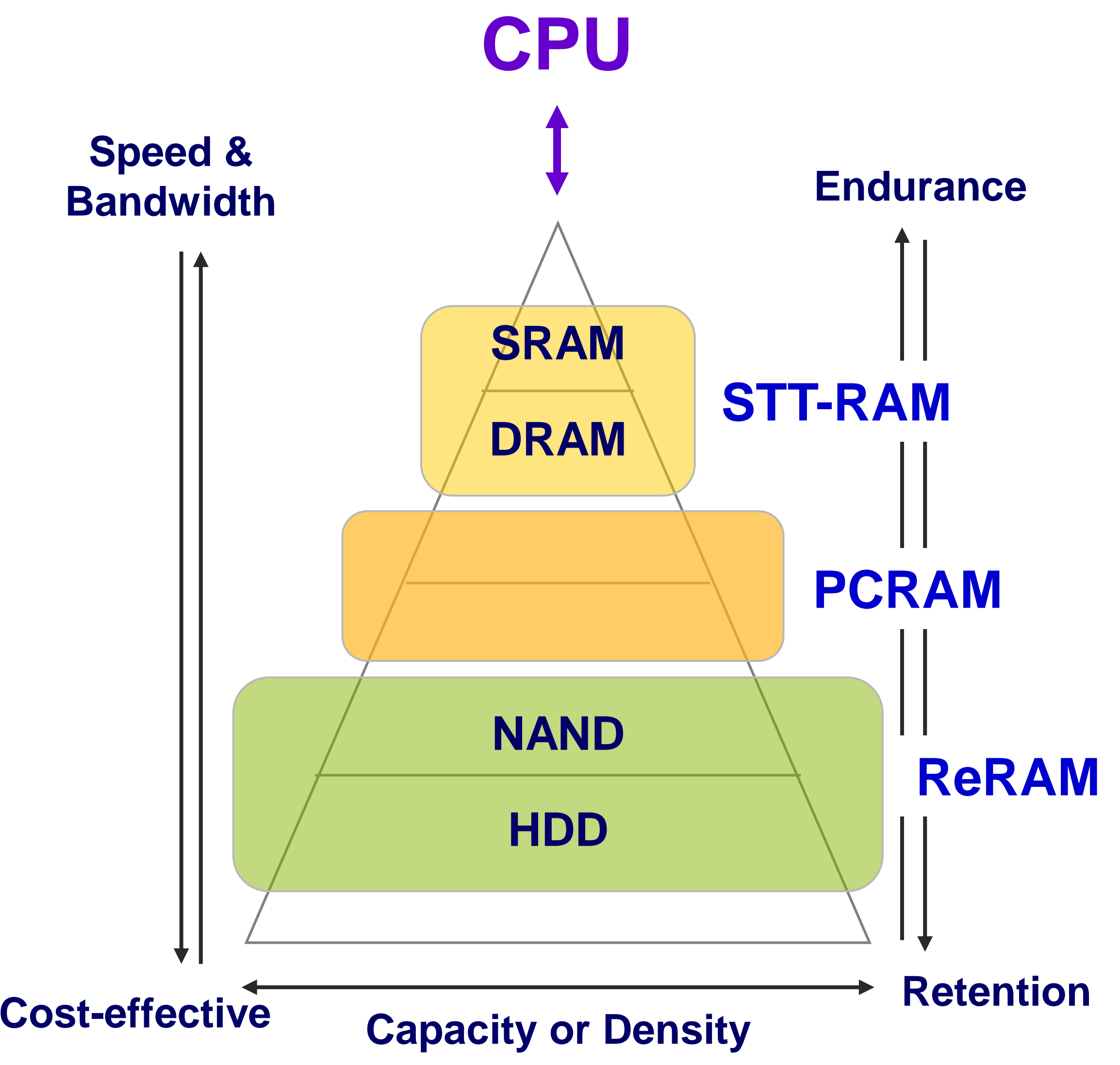
Schematic of 4-plane 8Mb ReRAM chip

1st Analog Decoder
col
row
Cell Array
Final Decoder underneath the cell
1st Digital Decoder
SA CTRL
Sense Amp.
Write Drv.



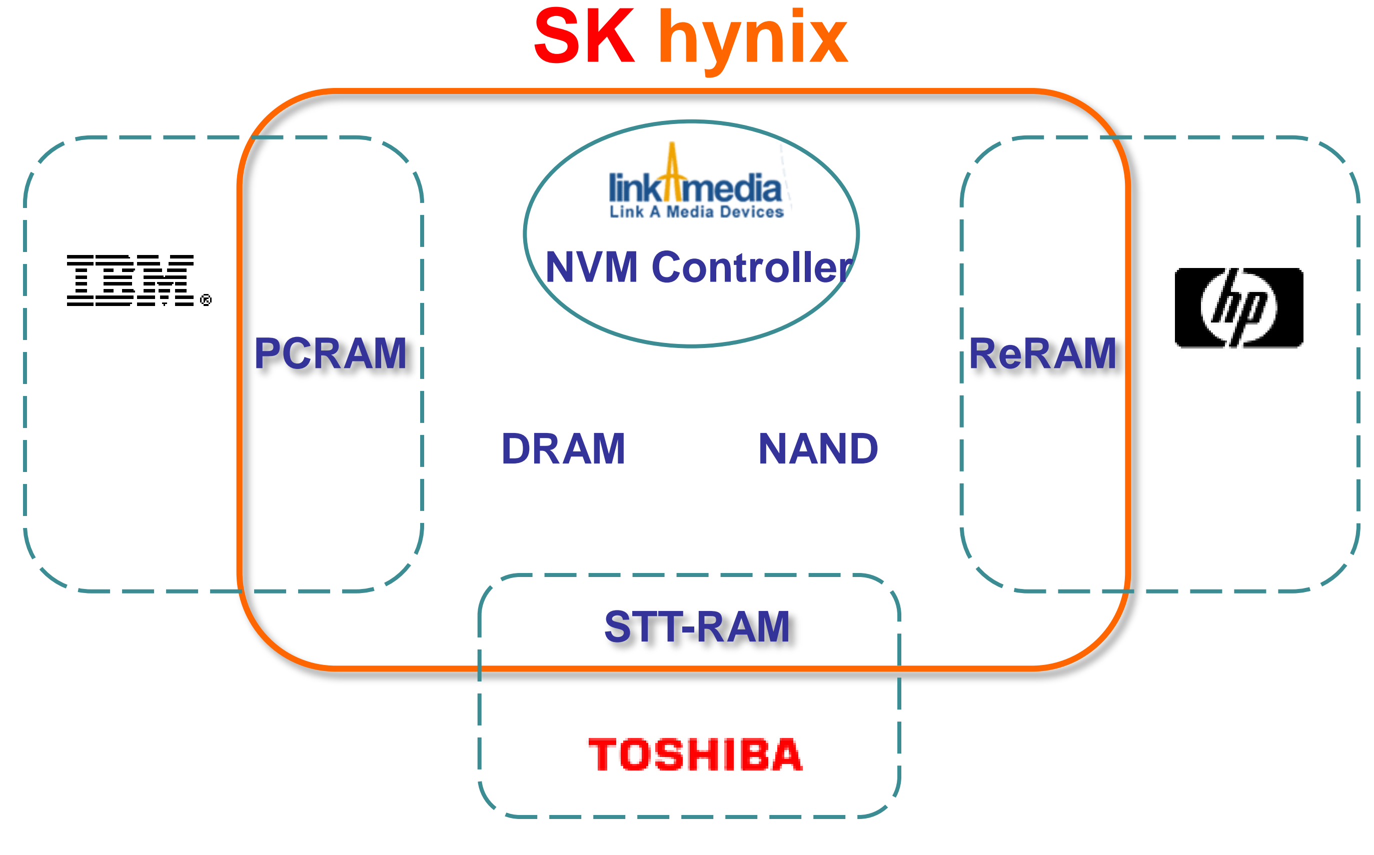
<Source : SOVT, USA 2012>

SK Hynix New Memory Strategy



New Memory Status in SK hynix

- Joint Development with IBM, HP, Toshiba
- Developing NVM Controller by Link A Media



Summary

- Cost effectiveness of 1xnm DRAM and NAND flash ?

- Developing Three types of New Memory
  - PCRAM, STT-RAM, ReRAM

- Possible Position of New Memory
  - PCRAM : SCM / Working Memory
  - STT-RAM : Working Memory / Cache Memory
  - ReRAM : Storage / SCM